3.3.1 Number of research papers published per teacher in the Journals notified on UGC CARE list during the years (2019-20)

S.No	Title of paper	Name of the author/s	Department of the teacher	Name of journal	Calendar Year of publication	ISSN number	Link to the recognition in UGC enlistment of the Journal /Digital Object Identifier (doi) number		
							Link to website of the Journal	Link to article / paper / abstract of the article	It is listed in UGC care list / Scopus / Web of Science / Other, mention
1	Multi – Precision Floating Point Arithmetic Unit design and implementation based on FPGA	Dr.S.KISHORE REDDY	ECE	The International journal of analytical and experimental modal analysis	2019	0886-9367	https://app.box.com/s/27gq8hv8kmzrkhvwhjf4xhh5lkc9q5u6	https://app.box.com/s/27gq8hv8kmzrkhvwhjf4xhh5lkc9q5u6	UGC care
2	Design and implementation of digital storage TRN Generator using FIFO and D-FF	Dr.S.KISHORE REDDY	ECE	International Journal of Research	2019	2236-6124	https://app.box.com/s/4cumn58ia6mvhnggyzyjd3t40c07bjzl	https://app.box.com/s/4cumn58ia6mvhnggyzyjd3t40c07bjzl	UGC care
3	Clock-gating of streaming applications for energy efficient implementations on FPGA's	Dr.S.KISHORE REDDY	ECE	The International journal of analytical and experimental modal analysis	2019	0886-9367	https://app.box.com/s/5fjw47y9e31tn9rq602q181p0a2vjb00	https://app.box.com/s/5fjw47y9e31tn9rq602q181p0a2vjb00	UGC care

PRINCIPAL
Avanthi Institute of Engg. & Tech
Gunthapally (V), Abdullapurmet (Mdl), R.R. Dist.

4	Design and implementation of deep learning neural networks based convolution and laplacian filter with image controlling on DLAU CONTROLLER	Dr.S.KISHORE REDDY	ECE	International Journal of Research	2019	2236-6124	https://app.box.com/s/mjodq3rnt13n5allgkjw3c1c7p79mvmf	https://app.box.com/s/mjodq3rnt13n5allgkjw3c1c7p79mvmf	UGC care
5	Clock-gating of streaming applications for energy efficient implementations on FPGA's	Dr.G.sai Kumar	ECE	The International journal of analytical and experimental modal analysis	2019	0886-9367	https://app.box.com/s/5fjw47y9e31tn9rq602q181p0a2vjb00	https://app.box.com/s/5fjw47y9e31tn9rq602q181p0a2vjb00	UGC care
6	Design and implementation of digital storage TRN Generator using FIFO and D-FF	Dr.G.sai Kumar	ECE	International Journal of Research	2019	2236-6124	https://app.box.com/s/4cumn58ia6mvhnggyzyjd3t40c07bjzl	https://app.box.com/s/4cumn58ia6mvhnggyzyjd3t40c07bjzl	UGC care
7	Multi - Precision Floating Point Arithmetic Unit design and implementation based on FPGA	Dr.G.sai Kumar	ECE	The International journal of analytical and experimental modal analysis	2019	0886-9367	https://app.box.com/s/27gq8hv8kmzrkhvwhjf4xhh5lkc9q5u6	https://app.box.com/s/27gq8hv8kmzrkhvwhjf4xhh5lkc9q5u6	UGC care
8	Design and implementation of deep learning neural networks based convolution and laplacian filter with image controlling on DLAU CONTROLLER	Dr.SAIKUMAR	ECE	International Journal of Research	2019	:2236-6124	https://app.box.com/s/mjodq3rnt13n5allgkjw3c1c7p79mvmf	https://app.box.com/s/mjodq3rnt13n5allgkjw3c1c7p79mvmf	UGC care
9	A novel approach of a Modified DCPET Based on Series Connection of Full-Bridge Converters	Mrs.E.PRASANNA	ECE	The International journal of analytical and experimental modal analysis	2019	0886-9367	https://app.box.com/s/z15wnbccuepukjix3fc89wavawd373d0	https://app.box.com/s/z15wnbccuepukjix3fc89wavawd373d0	UGC care

PRINCIPAL
Avanthi Institute of Engg. & Tech
Gunthapally (V), Abdullapurmet (Mdl), R.R. Dist.

10	A MPPT ALGORITHM BASED PV SYSTEM CONNECTED TO VOLTAGE CONTROLLED GRID	Mrs.E.PRASANNA	EEE	International Journal of Magazine	2019	2248-9278	https://www.scribd.com/document/694644802/A-Mppt-Algorithm-Based-Pv-System-Connected-To	https://www.scribd.com/document/694644802/A-Mppt-Algorithm-Based-Pv-System-Connected-To	UGC care
11	Control of DFIG Wind Power Generators in Unstable Microgrids founded in Instatnt Power Theory	Mr.S.SRIKANTH REDDY	EEE	International Journal For Innovative Engineering and Management Research	2020	2456-5083	https://www.ijiemr.org/public/uploads/paper/2567_approvedpaper.pdf	https://www.ijiemr.org/public/uploads/paper/2567_approvedpaper.pdf	UGC care
12	MITIATION OF VOLTAGE SAG USING DYNAMIC VOLTAGE RESTORER(DVR)	Mr.T.Kranthi Kumar	EEE	INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY	2020	2582-1431	https://www.ijeiat.com/images/sliders/ec6f2eb784f27d68288fa753ca73ca53.pdf	https://www.ijeiat.com/images/sliders/ec6f2eb784f27d68288fa753ca73ca53.pdf	UGC care
13	Cloud Consistency Maintaining As A Service Model For Auditing	Mr.P.Krishna Rao	CSE	International Journal of Innovations in Engineering and Technology (IJIET)	2020	2319-1058	https://ijiet.com/wp-content/uploads/2020/05/21.pdf	https://ijiet.com/wp-content/uploads/2020/05/21.pdf	UGC care
14	Cloud Consistency Maintaining As A Service Model For Auditing	Mr.T.Shravan	CSE	International Journal of Innovations in Engineering and Technology (IJIET)	2020	2319-1058	https://ijiet.com/wp-content/uploads/2020/05/21.pdf	https://ijiet.com/wp-content/uploads/2020/05/21.pdf	UGC care
15	Rule-based Mining of Juvenile Delinquency	Mrs.M.Shireesha	CSE	International Conference on Computer Communication and Informatics	2020	2329-7190	https://ieeexplore.ieee.org/document/9104126	https://ieeexplore.ieee.org/document/9104126	OTHER
16	Rule-based Mining of Juvenile Delinquency	Mr.S.Rajender	CSE	International Conference on Computer Communication and Informatics	2020	2329-7190	https://ieeexplore.ieee.org/document/9104126	https://ieeexplore.ieee.org/document/9104126	OTHER

PRINCIPAL
Avanthi Institute of Engg. & Tech
Gunthapally (V), Abdullapurmet (Mdl), R.R. Dist.

17	Rule-based Mining of Juvenile Delinquency	Mrs.A.Sravani	CSE	International Conference on Computer Communication and Informatics	2020	2329-7190	https://ieeexplore.ieee.org/document/9104126	https://ieeexplore.ieee.org/document/9104126	OTHER
18	Rule-based Mining of Juvenile Delinquency	Dr.Lalitha Saroja Thota	CSE	International Conference on Computer Communication and Informatics	2020	2329-7190	https://ieeexplore.ieee.org/document/9104126/authors#authors	https://ieeexplore.ieee.org/document/9104126/authors#authors	OTHER
19	PREREQUISITE OF ENGLISH LANGUAGE SKILLS FOR IT RECRUITMENT	Mrs.B. Nayeema	MBA	INTERNATIONAL JOURNAL OF RESEARCH IN EDUCATION AND PSYCHOLOGY (IJREP)	2019	2455-426X	https://doi.org/10.33329/IJREP.2019.48https://doi.org/10.33329/IJREP.2019.48	https://doi.org/10.33329/IJREP.2019.48https://doi.org/10.33329/IJREP.2019.48	UGC care
20	INFLUENCE OF ORGANISATIONAL CITIZENSHIP BEHAVIOUR FACTORS ON JOB SATISFACTION AMONG ENGINEERING COLLEGE TEACHERS IN ANDHRA PRADESH	Mrs.B. Nayeema	MBA	International Journal of Business and Administration Research Review	2020	2348-0653	https://junikhyatjournal.com/no_1_jun_20/19.pdf	https://junikhyatjournal.com/no_1_jun_20/19.pdf	UGC care
21	Design of Hybrid Energy Storage Systems in DC Microgrid Applications	Mrs.M.Ragini	EEE	INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY	2020	2582-1431	https://www.ijeiat.com/images/sliders/78d411a9652bd03ea0200eb034ef9393.pdf	https://www.ijeiat.com/images/sliders/78d411a9652bd03ea0200eb034ef9393.pdf	UGC care
22	Compensation of Harmonics and Dynamic Reactive Power with Grid Interconnection using Shunt Hybrid Active Power Filter Control Technique	Mrs.M.Ragini	EEE	INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY	2019	2582-1431	https://www.ijeiat.com/images/sliders/d26659722c5a7a96eff187b70cd4e1dd.pdf	https://www.ijeiat.com/images/sliders/d26659722c5a7a96eff187b70cd4e1dd.pdf	UGC care

PRINCIPAL
Avanthi Institute of Engg. & Tech
Gunthapally (V), Abdullapurmet (Mdl), R.R. Dist.

23	Compensation of Harmonics and Dynamic Reactive Power with Grid Interconnection using Shunt Hybrid Active Power Filter Control Technique	Mr.T.Kranthi Kumar	EEE	INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY	2019	2582-1431	https://www.ijeiat.com/images/sliders/d26659722c5a7a96eff187b70cd4e1dd.pdf	https://www.ijeiat.com/images/sliders/d26659722c5a7a96eff187b70cd4e1dd.pdf	UGC care
24	Aqaaaaaa Study Of Ultrasonic Metal Welding To Achieve Quality Welds	Mr.Ramesh babu Y	MECH	Journal of the Gujarat Research Society	2019	0374-8588	http://gujaratresearchsociety.in/index.php/JGRS/article/view/3974	http://gujaratresearchsociety.in/index.php/JGRS/article/view/3974	UGC care
25	competency analysis	Dr Y Jayapadha	MBA	International Journal ofMnagment	2020	0976-6502	https://iaeme.com/MasterAdmin/Journal_uploads/IJM/VOLUME_11_ISSUE_3/IJM_11_03_087.pdf	https://iaeme.com/MasterAdmin/Journal_uploads/IJM/VOLUME_11_ISSUE_3/IJM_11_03_087.pdf	UGC care
26	RSDQ MODEL OF 360 DEGREE FEEDBACK	Dr Y Jayapadha	MBA	International Journal of Management (IJM)	2020	0976-6502	https://iaeme.com/MasterAdmin/Journal_uploads/IJM/VOLUME_11_ISSUE_11/IJM_11_11_440.pdf	https://iaeme.com/MasterAdmin/Journal_uploads/IJM/VOLUME_11_ISSUE_11/IJM_11_11_440.pdf	UGC care
27	Performance Analysis and Practices	Dr Y Jayapadha	MBA	JOURNAL OF CRITICAL REVIEWS	2020	2394-5125	https://www.jcreview.com/admin/Uploads/Files/638c18cc42e993.41231179.pdf	https://www.jcreview.com/admin/Uploads/Files/638c18cc42e993.41231179.pdf	UGC care

PRINCIPAL
Avanthi Institute of Engg. & Tech
Gunthapally (V), Abdullapurmet (Mdl), R.R. Dist.

Multi - Precision Floating Point Arithmetic Unit design and implementation based on FPGA

G.MALATHI [1] DR.S.KISHORE REDDY[2] DR.G.SAI KUMAR[3]
malathig3006@gmail.com[1] kishorereddy416@gmail.com [2] saikumar418@gmail.com[3]
[1]PG Scholar, Dept of ECE,vlsi system design, Avanthi Institute of engineering and Technology,gunthapally, Ranga Reddy, Telangana.
[2]Associate Professor, HOD,Dept of ECE,vlsi design, Avanthi Institute of engineering and Technology gunthapally , Ranga Reddy, Telangana.
[3] Associate Professor, Dept of ECE, Avanthi Institute of engineering and Technology,gunthapally, Ranga Reddy, Telangana.

Abstract: Floating point math is very important in digital signal handling. Usually choosing separate floating point accuracy figures among different kinds of engineering apps, this leaves the floating point arithmetic device capable of operating on separate floating point accuracy figures. The fast advancement of FPGA technology allows for flexible design of arithmetic floating point. This paper describes how to construct a particular floating point arithmetic device using Verilog HDL depending on FPGA. A few double precision flying point figures or two full precision flying point figures operations can be introduced and subtracted. At the start of this paper, modeling and software tests demonstrate the features and calculation precision.

Index Terms—FPGA, multi precision floating point ,addition and substraction,IEEE 754.

I. INTRODUCTION

There is a need to process a large quantity of data with separate precision and powerful real-time specifications in digital signal processing, image analysis, voice communications, wireless communications and many other fields. Floating point math functions elevated precision. But contrary to arithmetic integer, arithmetic floating-point occupies more hardware funds to be applied by software in many apps. As a result, the working velocity of this floating point arithmetic is very small. And while arithmetic floating-point hardware can increase computational speed, multi-precision floating-point arithmetic requires many floating-point devices that pick up a large amount of hardware resources. Hardware expenses will be reduced if a floating point unit is constructed that can perform separate handling of precision. And the rapid development of FPGA allows it feasible. It was suitable to implement the floating point arithmetic within the floating point high-level languages; however, arithmetic hardware execution is a challenging job. The design of very large-scale computing (VLSI) software has become the most effective option for the implementation of flying point math systems due to its high storage volume, elevated performance, low price and versatile processing specifications. The IEEE 754 rule features two entirely distinct rotating point schemes, the binary interchange pattern and the decimal interchange pattern. This section relies with a single precision solely on uniform binary interchange method. Figure 1 demonstrates the depiction of a single-bit (S), eight-bit (E) and twenty-three-bit (M) or significant IEEE 754 full accuracy input code

II LITERATURE REVIEW

VFLOAT: A VARIABLE PRECISION FIXED- AND FLOATINGPOINT LIBRARY FOR RECONFIGURABLE HARDWARE

In variable precision floating-point library (VFloat) that supports general floating-point formats as well as IEEE standard formats. optimum reconfigurable hardware implementations could need the utilization of arbitrary floating-point formats that don't essentially adjust to IEEE standard sizes. Most antecedently printed floating-point formats to be used

with reconfigurable hardware square measure subsets of our format. Custom data paths with optimum bit widths for every operation may be designed mistreatment the variable exactitude hardware modules within the Float library, enabling a better level of similarity. The Float library includes three varieties of hardware modules for format management, arithmetic operations, and conversions between fixed-point and floating-point formats. The format conversions gives hybrid fixed- and floating point operations during a single style [1].

FAST, EFFICIENT FLOTING POINT ADERS AND MULTIPLIERS FOR FPGA

In implementation details for Associate an IEEE-754 floating-point adder Multiplier for FPGAs and FPU applications a growing trend within the FPGA community. As such, it's become vital to form floating-point units optimized for FPGA technology. the FPGA style area is completely different from the VLSI style space; so, optimizations for FPGAs will take issue considerably from optimizations for VLSI. specifically, the FPGA setting constrains the planning area such solely restricted similarity may be effectively exploited to scale back latency. Obtaining the correct balances between clock speed, latency, and space in FPGAs may be notably difficult. The styles given here modify a Xilinx Virtex4 FPGA (-11 speed grade) to attain 270 MHZ IEEE compliant double exactitude floating-point performance with a 9-stage adder pipeline and 14-stage multiplier pipeline. the world demand is close to 500 slices for the adder and beneath 750 slices for the multiplier [2].

SPEED-UP IN FPGA BASED BIT-PARALLEL MULTIPLIERS

This technique take into account the technology-dependent optimizations of fixed-point bit-parallel multipliers by completing their implementations by considering embedded primitives and macro support that are useful in modern-day FPGAs. FPGAs are the best option proving to be replacement of Application Specific Integrated Circuits (ASIC) primarily due to the low Non-recurring Engineering (NRE) prices related to FPGA platforms. This has prompted FPGA vendors to enhance the capability of the underlying primitive material and embody specialised macro support and material possession (IP) cores in their offerings. However, most of the work associated with FPGA implementations doesn't take full advantage of those offerings. Their implementation targets three completely different FPGA families viz. Spartan-6, Virtex-4 and Virtex5. The implementation results indicate that a substantial speed up in performance will occur these embedded FPGA resources.

A DUAL-MODE QUADRUPLE PRECISION FLOATING POINT DIVIDER

This section presents a multi-mode floating point multiplier operating efficiently with every precision format specified by the IEEE 754-2008 standard. The design performs one quadruple precision multiplication, or two double precision multiplications in parallel, or four single precision multiplications in parallel. The proposed multiplier is pipelined to achieve implementation of one quadruple multiplication in 3 cycles and either two double precision operations in similar or four single precision operations in similar in only 2 cycles. The planned design improves the throughput by a factor of two compared to a double precision multiplier and by four compared to a single precision multiplication. An example execution on VLSI verifies the plan and it achieves a maximum operating frequency of 505 MHz [4].

III.PROPOSED SYSTEM

The multi-precision floating-point arithmetic unit suggested in this document may alter the circuit's inner setup (when working), depending on the calculation accuracy, to accomplish single or double precision calculation with minimum hardware resources.

The multi-precision floating-point math efficiently converts a double-precision floating-point array into a few single-precision floating-point circuits[1]. Figure 1 shows its section diagram.

In Figure 1, DA, DB and DC are double-precision figures. a1, a2, b1, b2, c1 and c2 are single-precision figures. One of the following two activities may be implemented by the multii-precision floating-point arithmetic unit.

$$DC = DA \pm DB$$

$$c1 = a1 \pm b1, c2 = a2 \pm b2$$

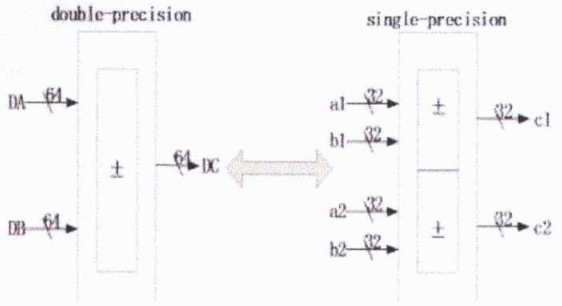


Figure 1.function schematic of multi precision floating point arithmetic

FLOATING-POINT REPRESENTATION

IEEE754 is the most commonly used rotating point range representation[2] and is shown in numbers 2(a) and (b) in its 32-bit single precision and 64-bit double precision data mode.

As shown in Figure 2, the column, the exponent, and the significand of the floating-point number must be gathered to represent a floating-point number. Eq is the true value of a set N floating-point. (1).In fact, a floating point number is a standardized real number consisting of the sign(S), the exponent(E) and the mantissa(M).

1bit	8bit	23bit
S(Sign)	Exponent(E)	M (Mantissa)

(a)single-precision floating-point number

1bit	11bit	52bit
S(Sign)	E(Exponent)	M (Mantissa)

(b)double-precision floating-point number

Fig 2 representation of a floating point number

$$N = (-1)^S \times 2^{E-Bias} \times (1.0 + M)$$

Note that the M in the Eq.(1) is the structured significand (the entire portion of the structured significand must be 1 and this 1 is voluntary and non-storage). Likewise, the actual outcome of the mobile point math must be taken to the uniform Eq.(1) size, meaning that the correct significand number must be 1. IEEE754 also sets out several unique information representations as shown in Table 1.

Table 1. Rrepresentation of special data

E	M	data
0	0	0
0	0	unnormalized number (Mantissa implication is 0)
All 1	0	INF(infinity)
1	0	NAN(not a number)

EXECUTION OF ARITHMETIC FLOATION-POINT

The extensive technique of incorporating and separating two flying point figures is divided into five phases, exponent pairing, significand calculation, significand normalization, significand counting, and overflow judgment[3]-[4]. The function of corresponding exponents is to match the standard positions of two speaking place figures; it is to match the reduced exponent with the larger exponent and transfer the speaking spot amount. The calculation of mantissas is to bring or subtract the mantissas based on the entry control signal.

significant normalization implies that the significant of the procedure consequence should fulfill the floating-point normalization criteria, that the entire portion should be 1. The exponent must make the respective addition and subtraction if the significand is shifted to the correct or to the left. The drawing of significand is to round off the data after shifting to the left of the scoring rule. When the exponent is overflowing or underflowing, the choice on overflow is to handle the operation result exponent. If the exponent overflows or outputs Machine zero of the floating point number, if the exponent underflows, it will output the infinite number form.

In addition to following the laws of floating point arithmetic, consideration should be given to designing a floating point arithmetic unit, saving hardware resource and enhancing operation velocity. Figure 3 demonstrates the internal floating point

framework arithmetic unit of multi-precision intended in this document.

As shown in Figure 3, the arithmetic unit consists mainly of six modules, the pre-processing module for data, the exponent comparison module, the significand stitching module, the addition module, the standardization and rounding processing module, and the module for overflow processing.

The two control signals in the scheme, Double and Op, should be illustrated before presenting the features of each module. Double is a selective information accuracy signal. When Double=1, double-precision arithmetic should be performed and the two 64-bit input data DA and DB are two double-precision floating-point numbers. When Double= 0, it performs single-precision arithmetic and the two 64-bit data as input A and B are four single-precision floating-point numbers representing the operation control signal a1, a2, b1 and b2.Op. If Op=0, the procedure should be added, while Op=1, the operation should be subtracted.

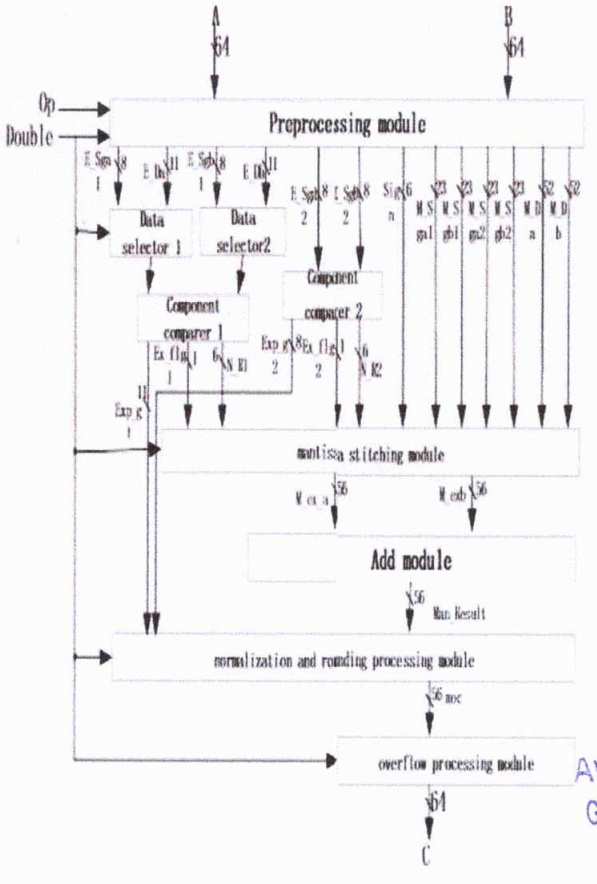


Figure3. Internal structure of the multi-precision floating-point arithmetic unit.

A.Pre-processing module

The preprocessing module offers information for later modules and performs the following three tasks primarily.

Divide the data sector. According to the Floatation-Point layout of Figure 1, entry information A of 64-bit should be split into 3 sections, floating-point range symbol, exponent and mantissa (a1 and a2) should be split into two precision single-point symbol, exponent and significand (b1 and b2), and output information of 64-bit B should be broken down into 3 sections. The symbol, exponent and significand of a DA floating point amount of double frequency disassemble A in three sections at the same moment. Similarly, B is disassembled into three parts by a symbol, exponent and decimal digits of another integer arithmetic number DB. In addition, the' 1', t should be indicated

Setting the flags of unique information. Setting up three flags, NAN, INF and ZERO (all 4 bits) of four singlle-precision floating-point numbers or two doubble— preecision floatiing-pointt numbers to determine the type of the two 64-bit input information according to 0, Plus or minus infinity and NAN in table 1.

Subtraction procedure pre-processing. If Op= 1, the operation of a bitwise NOT (negation) to the sign bits of b1, b2 and DB should be performed so that only the operation performed in subsequent modules can be added if no special data is available.

B. Exponent comparison module

The comparison module of the exponent compares a set of exponents of input. The ports, ia and ib import the exponents. And there are three OS, of ex and oN R output signals. OS is the larger performance exponent between ia and ib, namely the larger one. ON R is the absolute value of the distinction between two exponents and gives the correct significand shift step amount for the next module. Of ex is the flag of the swap. If of ex is equal to 1, showing ia < ib, the

mantissas of the two operands of a couple of operation numbers will be exchanged in the calculations that follow. On the contrary, if of ex is equal to 0, the significand must not be exchanged and the purpose of producing this signal is to always put the significand in DA / a1/a2, corresponding to the larger exponent of each pair of data. Therefore, it is only necessary to deal with DB / b1/b2 in the significand stitching module to move the significand to the right.

As shown in Figure 3, there are two comparison module exponent, exponent comparer 1and 2. And the information input in exponent comparer 1 comes from two information selectors. When Double is 0, the information is the a1 and b1 exponents. Data are the exponents of DA and DB when Double equals 1. And the exponent comparer 2 produces the outcome of a2 and b2 comparison. Significand

STITCHING MODULE

As shown in Figure 3, the significand stitching module has many input signals, including Double, significand swap flag, tiny exponent significand step number, four single-precision data symbols and mantissas, or two double-precision data. And this module's output is two 56-bit data.

This module understands splicing the significand into two Double Signal 56-bit information from four singlle-preecision information or two doubble-preecision data. The information after splicing is the complement method with two signs pieces to simplify the operating circuit. The larger significand exponent is located in DA / a1/a2, and the lower significand exponent is located in DB b1/b2 based along the magnitude of the exponent. The cause for the 56-bit significand is that when Double is equal to 1, the 53-bit significand is changed to a new 56-bit significand after adding an integer bit and two sign bits. In this manner, two distinct accuracy data can share one arithmetic unit. In addition, Figure 4 is the significand composition with distinct operational accuracy.

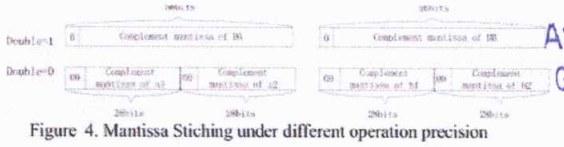


Figure 4. Mantissa Stiching under different operation precision

D. **The Sum Module Of The Mantissa Complement**

Because the sign of subtrahend has been disposed in

Table 2. Port signal of the mantissa normalization module

Name	name	width	Notes
input	doub	1	precision control
	iExp1	11	exponent 1
	iExp2	8	exponent 2
	iMan	56	Sum of mantissa
output	oData	64	operation result

When Op is equal to 1, the preprocessing module requires only two mantissas to add operation.

Because the significand to be summed is 56-bit, mostly the effects of the sum algorithm on the arithmetic speed[5]. The amount of significand has embraced a blended Han –Carlson[6] algorithm that trades room for moment, and its tree design has an edge over serial carry and look-ahead carry in the logical sequence, the cable channel, and the peak sector area. The heart of the Han-Carlson algorithm is the parallel prefix addition, and its three primary calculation steps are as follows.

Calculate the Pi and Gi of each augends bit and addend. And the Pi and Gi formula is displayed in Eq. (2) and (3) respectively.

$$P_i = A_i \cdot B_i \qquad (i=0\sim55) \qquad (2)$$

$$G_i = A_i \oplus B_i \qquad (i=0\sim55) \qquad (3)$$

(2) generate carry signal in parallel ,and the rule is shown in eq.(4)~eq.(6),in which the " ⊙"is the prefix operator.

$$C_i = G_{i\ldots\ldots0} + P_{I\ldots\ldots0}C_0 \qquad (4)$$

$$(G_{i\ldots0}, P_{\ldots i\ldots0}) = (G_{i-1}, P_{i-1}) \odot (G_{i-2}.P_{i-2}) \ldots\ldots\odot (G_0, P_0) \qquad (5)$$

$$(G_i, P_i) \odot (G_j.P_j) = (G_i + P_i \cdot G_j, P_i \cdot P_j) \qquad (6)$$

(3) calculate the sum of each bit ,and it is shown in eq.(7).

$$S_i = P_i \oplus C_i \qquad (7)$$

The A and B in eq.(2)~eq.(7)represent two 56-bit input data respectively. The Ai and Bi represent the

 ISSN NO: 0886-9367

ith bit of input data respectfully. And the Si and Ci represent the ith bit summation of their results and the carry input signal from

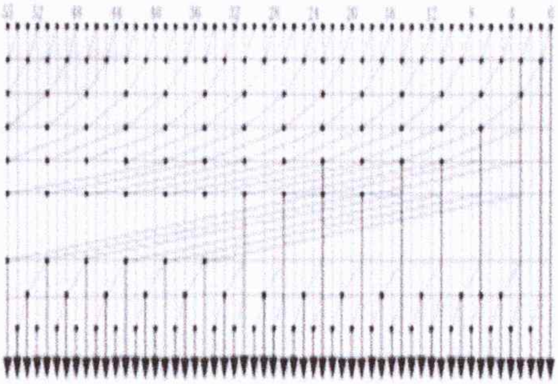


Figure5. The prefix operation of the 56-bit mixed Han-Carlson adder

Figure 5 is the inner structure of a 56-bit blended han-carlson adder[4], a space-for-time algorithm. Each input point is one (Gi, Pi), the binary addition method is split into nine phases. The black dots in the figure are a carrying operation and each bit's carrying bits are calculated at each point in parallel. Eventually, complete adder is used to calculate the outcomes of each bit.

Mantissa normalization module

G. The significant standardization module shifts the output significant of the addition module according to the precision requirement to a floating point numbers. Table 2 shows the input and output signals of this module.

This module comprises of three sub-modules that are the sub-module of the significant judgment, the leading sub-module of 0 identification and the sub-module of the processing of normalization.

The significant judgment sub-module prejudges the 56-bit complement significant before being normalized according to the dual signs and the highest numerical tad and get the symbol bit and the expedite which is the initial value of adding operation to the exponent and then to simplify the circuit, after significant has been transformed into the Sign-Magnit, subsequent processing will take place. The sub-module of the significant judgment primarily performs the following three tasks. Set the add operation offset, expedite, if exponent need not be shifted to the left, according to the dual sign-bits and the highest numerical bit of 56-bit complement mantissa. When expelling= 00, it means that the significant has been a standardized number already. If expedite=01, it reflects the adding exponent procedure with 1 (the significant equivalent moves 1 bit to the right). When expedite= 11, it represents that for several bits the significant needs to be shifted to the right, but the first 1 testing and coding module determines the numbers.

. Set the floating-point number sign bit.

Converting to absolute value the mantissa.

Leading the zero detection sub-module in significant normalization is the most time-consuming sub-module. The method of detection is first to determine which byte includes the largest bit "1" and then to encode the position of the first 1 by the priority encoder to provide significant with the left-shift numbers when normalized.

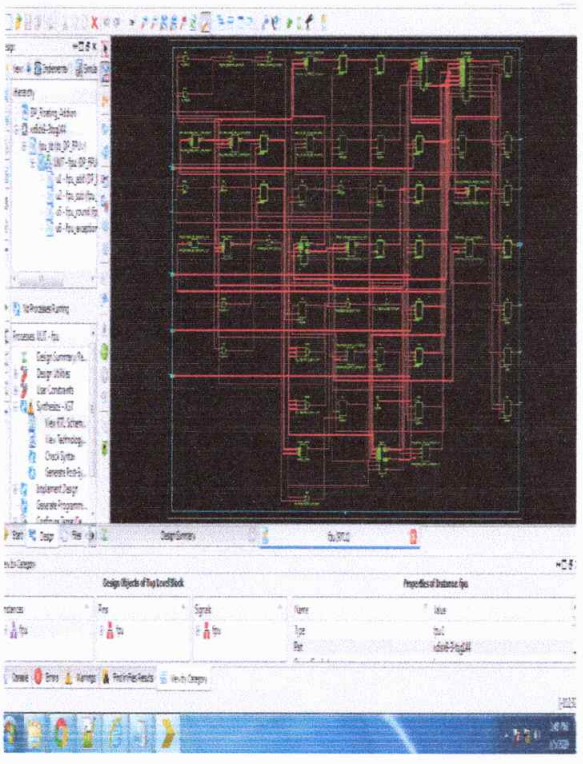
The sub-module for the processing of normalization passes the significant to the left or right according to the expedite value, and at the same moment adds or subtracts the exponents.

O. Rounding off and overflow judgment module The mantissa is rounded off according en route for the principle of the adjacent even-number by adding two numerical value bits in earlier for significant processing in this module, while the result of the proponent and significant are set accordingly in the case of exponent overflow. In other words, if the exponent underflows, the significant is set to 0 (representing floating point 0), if the exponent overflows, the exponent is set to all 1' and the significant is set to 0 (representing infinity).

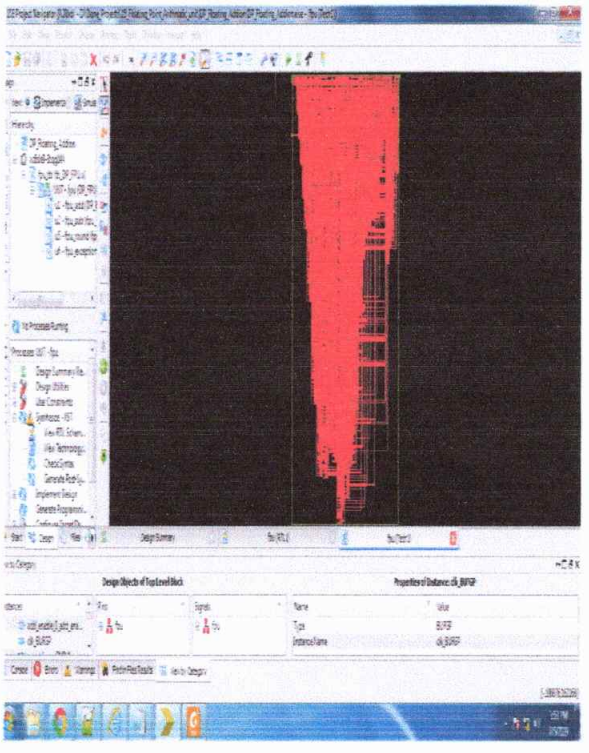
III. RESULTS

Experimental Results are shown for one of the applications is the intra MPEG-4 simple profile decoder. Due to restrictions on the number of clock buffers in Xilinx FPGAs, the design selected was trajectories to result in 32 actors.

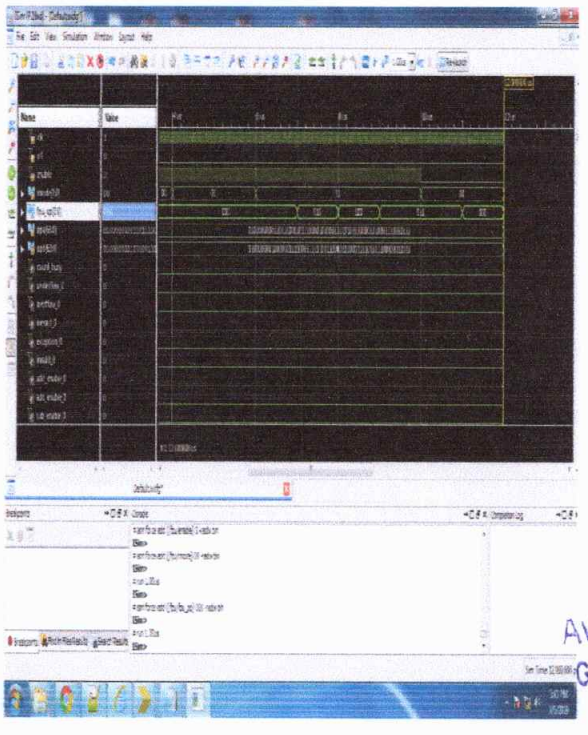
RTL SCHEMATIC:



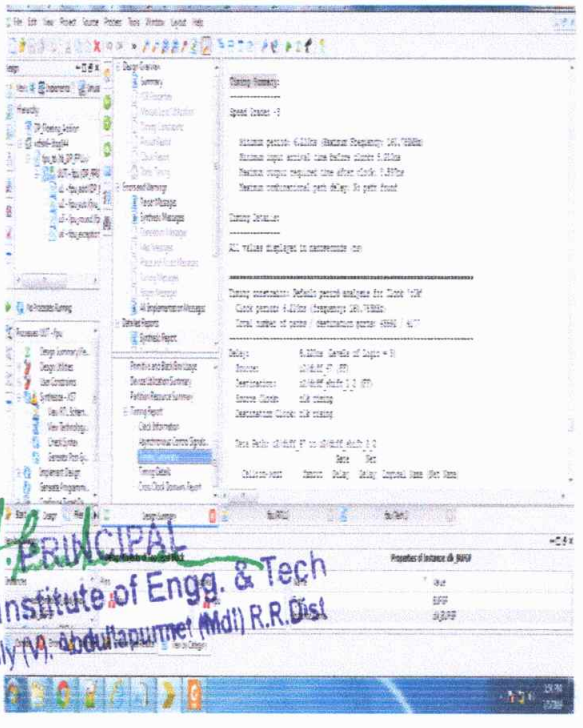
TECHNOLOGICAL SCHEMATIC



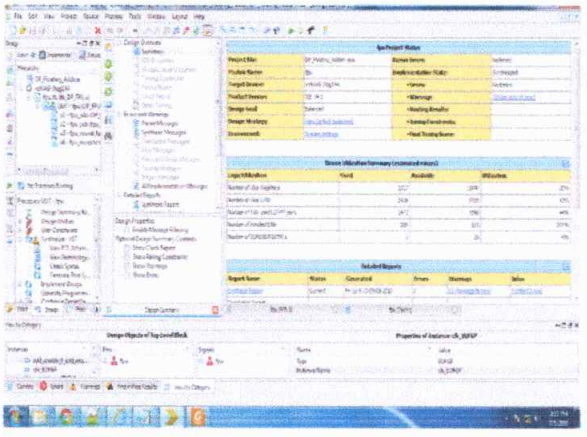
SIMULATION RESULT:



TIMING SUMMARY



DESIGN SUMMARY:



IV. CONCLUSION

The following paper proposed the layout of a floating point arithmetic multi-accuracy device, which could be used to combine or subtract single-precision two-group data or one-group floating point data with power signals entry. This paper proposed The system uses hardware funds quickly and less quickly in computing. These features are confirmed by both software simulation and experimentation..

REFERENCES

[1] M. Pedram, "Power minimization in IC design: Principles and applications," ACM Trans. Design Autom. Electron. Syst., vol. 1, no. 1, pp. 3–56, Jan. 1996. [Online]. Available: http://doi.acm.org/10.1145/225871.225877

[2] Q. Wu, M. Pedram, and X. Wu, "Clock-gating and its application to low power design of sequential circuits," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 47, no. 3, pp. 415–420, Mar. 2000.

[3] G. E. Tellez, A. Farrahi, and M. Sarrafzadeh, "Activity-driven clock design for low power circuits," in IEEE/ACM Int. Conf. Comput.-Aided Design Dig. Tech. Papers (ICCAD), San Jose, CA, USA, Nov. 1995, pp. 62–65.

[4] E. A. Lee and A. Sangiovanni-Vincentelli, "Comparing models of computation," in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Austin, TX, USA, 1997, pp. 234–241.

[5] G. Kahn, "The semantics of simple language for parallel programming," in Proc. IFIP Congr., Stockholm, Sweden, 1974, pp. 471–475.

[6] E. A. Lee and D. G. Messerschmitt, "Static scheduling of synchronous data flow programs for digital signal processing," IEEE Trans. Comput., vol. 36, no. 1, pp. 24–35, Jan. 1987.

[7] E. A. Lee and T. M. Parks, "Dataflow process networks," Proc. IEEE, vol. 83, no. 5, pp. 773–801, May 1995.

[8] S. Suhaib, D. Mathaikutty, and S. Shukla, "Dataflow architectures for GALS," Electron. Notes Theor. Comput. Sci., vol. 200, no. 1, pp. 33–50, 2008.

[9] T.-Y. Wuu and S. B. K. Vrudhula, "Synthesis of asynchronous systems from data flow specification," Inf. Sci. Inst., Univ. Southern California, Los Angeles, CA, USA, Tech. Rep. ISI/RR-93-366, Dec. 1993.

[10] B. Gravamen and H. Pedram, "High performance asynchronous design flow using a novel static performance analysis method," Comput. Elect. Eng., vol. 35, no. 6, pp. 920–941, Nov. 2009.

[11] S. C. Brunet et al., "Partitioning and optimization of high level stream applications for multi clock domain architectures," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 2013, pp. 177–182.

[12] S. Casals-Brunet, "Analysis and optimization of dynamic dataflow programs," Ph.D. dissertation, STI Elect. Eng., STI, Lausanne, Switzerland, 2015.

[13] E. Bezati, "High-level synthesis of dataflow programs for heterogeneous platforms," Ph.D. dissertation, STI, Lausanne, Switzerland, 2015.

[14] S. Casual-Brunet, M. Mattavelli, and J. W. Janneck, "Buffer optimization based on critical path analysis of a dataflow program design," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Beijing, China, May 2013, pp. 1384–1387.

[15] Analysis of Power Savings from Intelligent Clock Gating, Xilinx, San Jose, CA, USA, Aug. 2012.

[16] (2014). Open RVC-CAL Applications. Accessed on Feb. 25, 2014. [Online]. Available: http://github.com/orcc/orc-apps

[17] M. Canale, S. Casals-Brunet, E. Bezati, M. Mattavelli, and J. Janneck, "Dataflow programs analysis and optimization using model predictive control techniques," J. Signal Process. Syst., vol. 84, no. 3, pp. 371–381, 2015. [Online]. Available: http://dx.doi.org/10.1007/s11265-015-1083-4

G.MALATHI was born on July 12th, 1996, completed her graduation in Electronics and communications Engineering from SLC's college .Currently she is pursuing M.Tech in vlsi system design from Avanthi Engineering College. Her areas of interest include vlsi and system design.

Prof.Dr.S.KISHORE REDDY working as an associate professor in the Dept of Electronics and communication at Avanthi Engineering College. He received his bachelor degree and master's degree from Jawaharlal Nehru Technological University Hyderabad, Kukatpally, India. Currently he is completed his PH.D.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Design and implementation of digital storage TRN Generator using FIFO and D-FF

[1]Shajahan, [2]Dr.S. Kishore Reddy, [3]Dr.G.sai Kumar

[1]M.Tech student ECE , VLSI system design. Avanthi institute of engg & tech.

E mail : sajumhod08525@gmail.com

[2]Associate professor,HOD ECE , VLSI design Avanthi institute of engg & tech.
E mail : kishorereddy416@gmail.com

[3]Associate professor ECE Department. Avanthi institute of engg & tech.
E Mali: saikumar418@gmail.com

ABSTRACT

Cryptographic frameworks have turned into an indispensable piece of our day by day life through the need of security exercises, for example, correspondence, electronic cash frameworks, and plate encryptions. Irregular numbers is a key segment for fortifying and verifying the secrecy of electronic interchanges and utilized in numerous cryptographic applications like key age, encryption, concealing conventions, web betting. Eccentric arbitrary numbers are fundamental for the security of cryptographic calculations for creating the hidden mystery keys. Genuine irregular number generators (TRNGs) have turned into an indispensable part in numerous cryptographic frameworks, including PIN/secret word age, confirmation conventions, key age, arbitrary cushioning, and nonce age. The circuit uses unsure irregular procedure, more often than not as electrical clamor, as an essential source. Field programmable entryway exhibits (FPGAs) structure a perfect stage for equipment executions of a significant number of these security calculations. Proposed TRNG depends on the guideline of beat recurrence identification for Xilinx-FPGA-based applications.

1. INTRODUCTION TO RANDOM GENERATORS:

In this day and age security is of most elevated significance and henceforth cryptography assumes a significant job in PC and systems administration security. Cryptography is a lot of procedures for concealing data. It is utilized in a few fields as a major aspect of security conventions to verify ordered data and information. Correspondence, being an indispensable piece of life, including the web and different methods for correspondence has offered ascend to security dangers. Cryptography along these lines gives the vital insurance from the dangers by ensuring the information, for example giving various methods and techniques for changing over information into an indistinguishable structure. The essential point of cryptography is that the unapproved client can't got to information. The substance of the information edges ought to be encoded with unmistakable example. Another application is to guarantee that the information should dependably be recognized by the originator of the message. Arbitrary numbers are fundamental to security in light of the fact that cryptographic frameworks rely upon the presence of some mystery information known to approved clients and capricious by others and regularly irregular strings are utilized to warrant its unconventionality (e.g., in keys, salts, ounces, challenges, instatement vectors, and other one-time quantities)[1]. Cryptographically ensured arbitrary number generators are significant for this reason. An irregular number generator is a computational gadget intended to create a series of numbers. Strategies for producing arbitrary has been utilized from old occasions, including dice, coin flipping, the rearranging of playing a game of cards, the utilization of yarrow stalks, and numerous different systems. There are number of arbitrary number age plans and Random Number Generators effectively utilized in IT security items. The arbitrary numbers created ought to be genuinely irregular, else they can essentially debilitate the security framework. They should eccentric. It must be planned with a decent cryptographic quality. It ought to be consistently disseminated on a given range and ought not be reliant on one another. Accordingly there is a requirement for a perfect RNG that fulfills every one of these prerequisites [3].Cryptographic quality is accomplished by arbitrary numbers that fulfill the necessities of cryptographic calculations. Irregular

number generators can be delegated either pseudo arbitrary number generators or genuine arbitrary number generators. A pseudo arbitrary number generator creates a flood of numbers that seems, by all accounts, to be irregular yet really pursue predefined grouping. A genuine arbitrary number generator creates a flood of erratic numbers that have no characterized pattern[3].

Genuine Random Number Generators: There are three ordinarily utilized strategies, in particular (i)oscillator examining, (ii)direct enhancement and (iii)discrete time mayhem. In the oscillator examining approach, period transformations (for example oscillator jitter) in a low recurrence clock of low quality factor (Q) is created by utilizing it to test a high recurrence clock. The immediate enhancement procedure digitizes warm or shot commotion, utilizing an intensifier and comparator. At long last, disorderly frameworks can be utilized to create TRNGs[11]. It is notable that beginning with a decent numerical idea (like a LFSR), somebody can construct an arbitrary number generator, called a Pseudo Random Number Generator (PRNG), acquiring a similar haphazardness test results as a decent True Random Number Generator (TRNG). In this generator yield is an element of the past one. In the vast majority of the cases it can turn into the best helplessness of the entire cryptographic framework. This is the reason a TRNG comprises of three primary parts as depicted in Fig. 1.

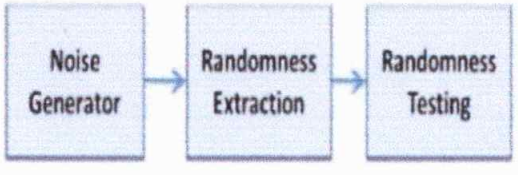


Fig 1. Main components of TRNG

The clamor generator is the black box utilized for producing arbitrary groupings. It depends on various sort of physical flighty marvel, as inestimable radiations, oscillators jitter, sound and light proliferation all through various conditions, and so on. The irregularity extraction box is utilized to help the generator to consistently appropriate the 0 and 1 bits along the output[2].The Randomness Testing square comprises of a lot of measurable tests, utilized for testing the haphazardness of the yield. The last two squares depend on simply numerical ideas.

1.1. Pseudorandom Number Generators:

There are various methods to make pseudorandom progressions, and the customary programming based systems, which would all be able to be completed in gear. A regular strategy for making a PRNG is to use the yield of a straight analysis move register (LFSR).The direct info move register (LFSR) is a run of the mill structure frustrate for executing a pseudo-subjective number generator (PRNG) since it might be negligibly created from a movement of fell flip-flops and a couple XOR portals. In any case, the LFSR is ordinarily inadequate without any other person's contribution for making surprising sporadic number courses of action. Its straight lead allows an encryption key to be successfully recovered in case it is used as keystream generator [8]. Disregarding the way that this methodology has extraordinary quantifiable properties and prompts extraordinarily beneficial hardware utilization, the Berlekamp–Massey figuring can be used to capably discover the affiliation polynomial from the LFSR"s yield gathering, making it unsuitable for cryptographic applications.

Classes of TRNG:

There are two fundamental classes of TRNG are

(I) Thermal clamor based and

(ii) Chaotic circuit based as appeared in Fig 2.

(i) The warm tumult generator heightens the noise made by electrons spilling into a resistor and changes over the racket to a discretionary number. The sign level of the warm uproar is underneath 1mV, making this approach progressively helpless against cutting edge trading commotion implantation (not sporadic, data subordinate) in an enormous scale SoC. In any case, the wellspring of clatter used in the warm RNG (foundation commotion by electron moving in the resistor) is extremely sporadic and adds to the power of the TRNG.

(ii) (ii) A scattered TRNG mishandles the strange thought of disarranged oscillators to create sporadic numbers. Progression in the nonlinear structure theory exhibited that noisy circuits can be seen as extremely self-assertive. The sign level in a scattered oscillator can be made much higher than in the warm TRNG. Consequently the Signal to Noise Ratio (SNR) is improved, constraining data dependence. As far as possible the effect of supply and substrate clatter by joining the 2 noncorrelated yields of

both TRNG with a XOR entryway (Figure 1) and besides by circuit techniques like falling. Since the trade work from the supply to the yield is various for each circuit and the 2 TRNG use unmistakable tumult sources to make the discretionary bits, the 2 bit streams are not connected .

2. LITERATURE REVIEW:

FPGA is used continuously because of its focal points in execution, plan time, control usage, versatility, cost or chip area over various structures reliant on microchip, DSP or VLSI. With a FPGA-based self-assertive number age, various cryptographic applications can be sufficiently realized using FPGA. Consistently, various TRNGs have been proposed.

For example, Tsoi and Leung proposed a FPGA-set up together TRNG based concerning the oscillator stage clatter. In their recommendation, an astounding sporadic piece stream can be delivered by looking at an exact high-repeat clock using a ring oscillator confined by entryways in the FPGA together with external resistors and capacitors. In any case, the most extraordinary yield date rate of the generator is simply 4.7Kbps which isn't adequately high for some cryptographic applications. In addition, the TRNG can be viably modified in light of the fact that it has external parts.

n Epstein and Harsa TRNG reliant on modernized circuit metastable event was shown. Nevertheless, the proposed generator must be viably realized in some low end progressed consolidated circuits anyway not in present day FPGAs in light of the way that CMOS circuits in current FPGAs are quick to the point that the probability of a metastable event occurring in any entryway in the FPGAs is close to nothing. Reconfigurable contraptions have transformed into an essential bit of many embedded automated systems, foreseen to transform into the phase of choice for general enlisting within the near future. Being fundamental prototyping contraptions, reconfigurable systems including FPGAs are by and large connected with cryptographic applications, as they can offer qualified to high taking care of rate at much lower cost and faster structure process length [4].

FPGAs being versatile to the extent programming and utilization of a couple of estimations and limits have been used for completing cryptographic figurings for a genuine long time. They are comprehensively used in encryption and R&D applications. FPGAs give execution versatility and points of interest being stood out from applications express planned circuit (ASICs). Usually, ASICs was used more for the cryptographic utilization [3].

A while later, on account of increasingly unmistakable flexibility and recreate limit, it has ended up being more straightforward to change estimations and program them on FPGAs. The improvement of an estimation is faster and mulls over a shorter time to exchange on FPGA. Focus is to design an improved field-programmable passage group (FPGA) based TRNGs, using completely propelled fragments. Using automated structure impedes for TRNGs has the great position that the plans are modestly essential and suitable to the FPGA arrangement stream, as they can sensibly utilize the CAD programming mechanical assemblies available for FPGA structure. In any case, mechanized circuits show almost set number of wellsprings of sporadic upheaval, e.g., metastability of circuit segments, repeat of free running oscillators, and butterflies (self-assertive stage shifts) in clock signals. Because of its flexibility and fast time to publicize, FPGA has transformed into a notable stage for realizing various cryptographic systems that fuse TRNGs as a fundamental square. It is fundamental to become new FPGA TRNG courses of action since: (I) not all the gear TRNG systems open for ASICs or various stages are flexible to FPGA execution; (ii) the current FPGA TRNGs have a couple of insufficiencies to the extent the throughput-per-unit-region and can be improved; and (iii) unique part strikes similarly as changes in operational conditions, for instance, assortments in temperature and voltage supply may inclination and irritate the sporadic property TRNGs yield bitstream. Since a huge part of the TRNGs work in an open-circle style, it is basic to combine a segment to ceaselessly offer an analysis hint to adaptively alter the TRNG system parameters to extend its yield bit randomness[7].

A moderately ongoing upgrade to FPGA abilities is Dynamic Partial Reconfiguation (DPR) or Runtime Partial Reconfiguration (RPR). It is the capacity to adjust (for the most part through the expansion of usefulness) the current circuit on the FPGA, through "fractional reconfiguration" (PR) of the FPGA at run time. DPR enables creator to utilize littler gadgets, lessen control utilization and improve framework upgradability. DPR enables adjustments to predefined parts of the FPGA rationale texture on-the-fly, without influencing the typical usefulness of the FPGA. TRNG circuit execution for Xilinx-FPGA-based applications, which has a tunable jitter control ability dependent on powerful fractional reconfiguration (DPR) accessible on Xilinx FPGAs. Plan procedures exist to anticipate any malevolent

controls through DPR which in different ways may influence the security of the framework named as Hardware Trojan Insertion [4].

Irregular number generators have applications in betting, factual examining, PC recreation, cryptography, totally randomized plan, and different regions where creating a flighty outcome is attractive. For the most part, in applications having unconventionality as the foremost, for example, in security applications, equipment generators are commonly favored over pseudo-irregular calculations, where attainable. Irregular number generators are extremely valuable in creating Monte Carlo-strategy recreations, as troubleshooting is encouraged by the capacity to run a similar succession of arbitrary numbers again by beginning from a similar arbitrary seed. They are likewise utilized in cryptography – inasmuch as the seed is mystery. Sender and collector can produce indistinguishable arrangement of numbers consequently to use from keys.

The age of pseudo-irregular numbers is a significant and normal errand in PC programming. While cryptography and certain numerical calculations require an exceptionally high level of evident arbitrariness, numerous different tasks just need an unobtrusive measure of capriciousness. Some straightforward models may give a client an "Arbitrary Quote of the Day", or figuring out what direction a PC controlled foe may move in a PC game. More fragile types of arbitrariness are utilized in hash calculations and in making amortized looking and arranging calculations.

A few applications which show up at first sight to be appropriate for randomization are in certainty not exactly so straightforward. For example, a framework that "haphazardly" chooses music tracks for a mood melodies framework should just seem arbitrary, and may even have approaches to control the choice of music: a genuine irregular framework would have no confinement on a similar thing seeming a few times in progression.

There are two head techniques used to create arbitrary numbers. The main technique estimates some physical marvel that is relied upon to be arbitrary and afterward makes up for potential predispositions in the estimation procedure. Model sources incorporate estimating climatic commotion, warm clamor, and other outer electromagnetic and quantum wonders. For instance, grandiose foundation radiation or radioactive rot as estimated over short timescales speak to wellsprings of regular entropy.

The speed at which entropy can be reaped from common sources is subject to the basic physical marvels being estimated. Along these lines, wellsprings of normally happening "genuine" entropy are said to square – they are rate-constrained until enough entropy is reaped to satisfy the need. On some Unix-like frameworks, including most Linux disseminations, the pseudo gadget document/dev/arbitrary will obstruct until adequate entropy is collected from the environment.[1] Due to this blocking conduct, huge mass peruses from/dev/irregular, for example, filling a hard circle drive with irregular bits, can frequently be moderate on frameworks that utilization this sort of entropy source.

3. PROPOSED DESIGN FOR TRN GENERATOR USING FIFO AND D-FF:

3.1 DESIGN OVERVIEW:

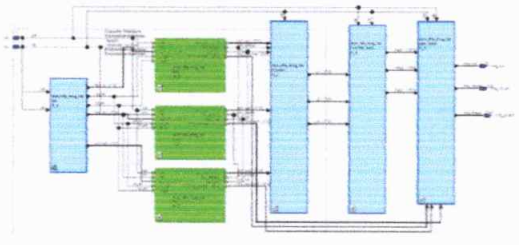
Genuine irregular numbers and physical nondeterministic arbitrary number generators (RNGs) appear to be of a regularly expanding significance. Arbitrary numbers are fundamental in cryptography (scientific, stochastic, and quantum), Monte Carlo counts, numerical recreations, measurable research, randomized calculations, lotteries, and so forth. Today, genuine irregular numbers are most fundamentally required in cryptography and its various applications to our regular day to day existence: versatile correspondences, email get to, online installments, cashless installments, ATMs, e-banking, Internet exchange, purpose of offer, prepaid cards, remote keys, general digital security, conveyed control network security (SCADA), and so forth. In cryptography, where because of Kerckhoffs' standard all pieces of conventions are freely known with the exception of some mystery (the key or other data) known uniquely to the sender and the beneficiary, unmistakably the mystery must not be measurable by a busybody, i.e., it must be arbitrary. Genuine RNGs are for the most part built with the end goal that the relationship among bits is little which the possibility of haphazardness is, specifically,. At times the physical framework that is estimated is being "reset" to an underlying condition after generation of each piece so as to decrease autocorrelation. In this way much of the time just a couple of most reduced request autocorrelation coefficients are noteworthy, in a perfect world just the first, which is named autocorrelation and meant by a. There are a lot of developments of genuine RNGs and research is as yet getting impulse, yet in our view one can generally order the present workmanship into four families:

• Noise-based RNGs

- Free-running oscillator RNGs
- Chaos RNGs
- Quantum RNGs

The tree of RNGs is delineated in Fig. 1. Scientific, pseudorandom generators can likewise be isolated into a few classifications relying upon the sort of calculation utilized.

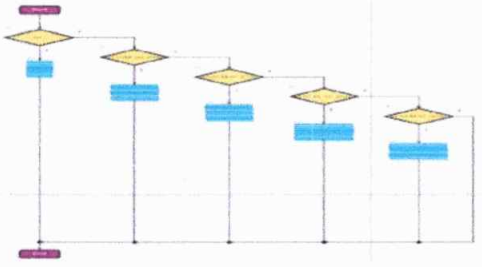
The significant commitment of this brief is the improvement of a design which permits on-the-fly legitimacy of factual characteristics of a TRNG by using DPR abilities of present day FPGAs for shifting the advanced clock director (DCM) displaying parameters. As far as we could possibly know, this is the main announced work which consolidates validity in a TRNG. This methodology is material for Xilinx FPGAs which give programmable clock age system and capacity of DPR. DPR is a moderately new upgrade in FPGA innovation, whereby changes to predefined bits of the FPGA rationale texture are conceivable on-the-fly, without influencing the typical usefulness of the FPGA. Xilinx clock the board tiles (CMTs) contain a dynamic reconfiguration port (DRP) which permits DPR to be performed through a lot less difficult methods. Utilizing DPR, the clock frequencies produced can be changed on the fly by altering the relating DCM parameters. DPR by means of DRP is an additional bit of leeway in FPGAs as it enables the client to tune the clock recurrence according to the need. Structure strategies exist to avoid any vindictive controls through DPR which in different ways may adversely influence the security of the framework. The objective of this brief is the structure, examination, and execution of a simple to-plan, improved, low overhead, and tunable TRNG for the FPGA stage.



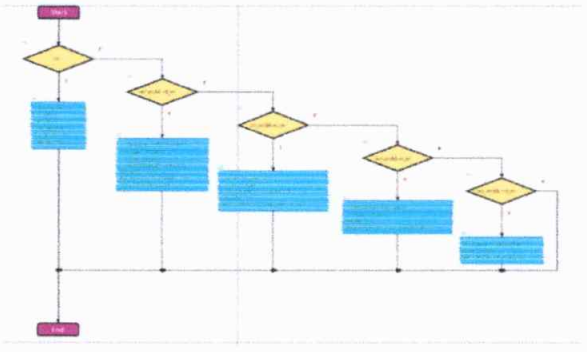
This modeling of the design is observed from the each synchronizer response of the mean time failure and its PAD parameters. Since the existing design models (mentioned III) would suffice the real time aspects parametric criteria which would impart correct scenario for the model and its enhancements based on its.Hence, we utilize this section of design model to implement the enhanced version of the synchronizer utilized. Our aim to provide the data and its implementation on the design modules which would results in correct output which is observed on the same synchronized cycle.

FLOW DIAGRAMS FOR PROPSED DESIGN:

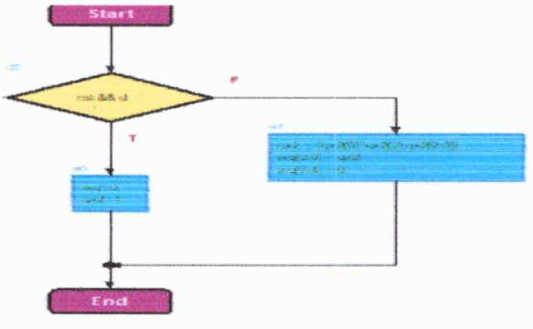
FLIP FLOP DESIGN FLOW:

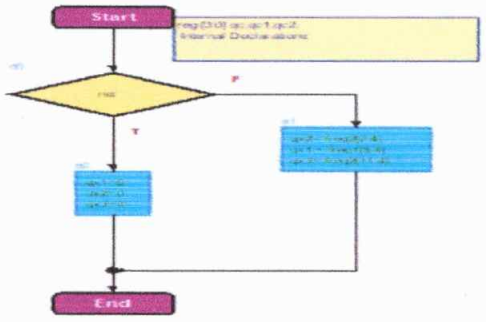


FIFO DESIGN FLOW:

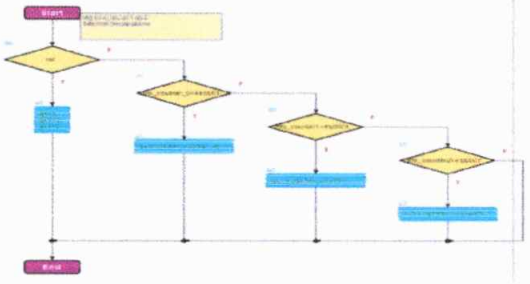


LFSR DESIGN FLOW:





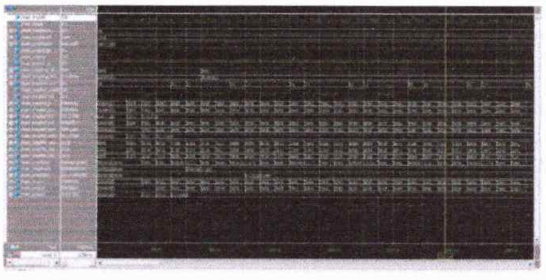
COUNTER DESIGN FLOW:



DISCUSSIONS:

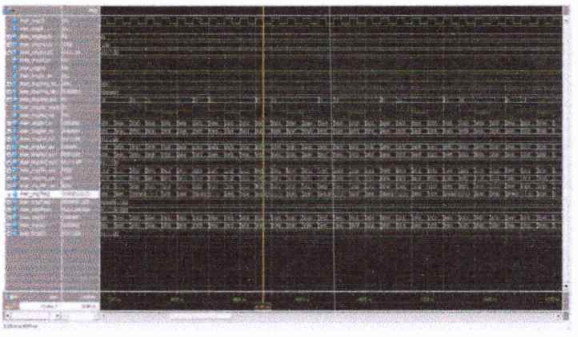
1. We have proposed the block diagram as mention in figure 4.1 stating different modules design aspects changes from the existing design scenario.
2. Now, from the above modules flow diagram we can estimate accuracy on hardware tool Xilinx which would provide the design platform to analyze the area, power and delay analysis.
3. The simulation was perceived by Model sim software which provides the correct framework output for the design chosen.
4. In our design, we have utilized FIFO and LFSR for better randomness and synchronization which enhances the output credibility outstandingly on area or power.

4. RESULTS AND DISCUSSIONS:



Our design framework on simulations would realize on the different buf_out values observed from the design choosen. Here depending on the LFSR seed values {input, input1 and input2} would vary the outputs observed at LFSR output. Each output from LFSR is synchronized on FIFO with read and write operation to have the design criteria for better PASD {power, area, speed and delay}.

Now these synchronized data are utilized with flip flop and counter to generate specific key frequencies and its key_values for better accuracy. Based on the different values from the LFSR seed we could estimate the different values of the true random generator output.



SYNTHESIS REPORT:

AREA UTILIZATION:

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Latches	4	178,176	1%
Number of 4 input LUTs	14	178,176	1%
Number of occupied Slices	7	89,088	1%
Number of Slices containing only related logic	7	7	100%
Number of Slices containing unrelated logic	0	7	0%
Total Number of 4 input LUTs	14	178,176	1%
Number of bonded IOBs	8	960	1%
IOB Latches	4		
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.63		

FIFO UTILIZATION

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	357	178,176	1%
Number of 4 input LUTs	704	178,176	1%
Number of occupied Slices	395	89,088	1%
Number of Slices containing only related logic	395	395	100%
Number of Slices containing unrelated logic	0	395	0%
Total Number of 4 input LUTs	736	178,176	1%
Number used as logic	704		
Number used as Route-thrus	32		
Number of bonded IOBs	69	960	7%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	4.69		

An estimation for the area and the power have been tabulated as shown above figures 1:2, and for power 3:4. Now, as we know that with use of the LUT minimization algorithm in address scheme storage for the design parameters we could estimate the performance as shown. T

POWER UTILIZATION:

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	9.05	3	---	---
Logic	0.00	14	178176	0
Signals	0.00	31	---	---
IOs	0.00	8	960	1
Quiescent	1344.28			
Total	1353.33			

LFSR POWER UTILIZATION

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	83.87	1	---	---
Logic	0.00	736	178176	0
Signals	0.00	635	---	---
IOs	0.00	69	960	7
Quiescent	1350.88			
Total	1434.75			

Similarly, we had estimated the design for the different logical units such as multiplier where each module would estimate the power characteristics based on the clk applied on the respective module.

CONCLUSIONS:

We have displayed an enhanced completely advanced tunable TRNG for FPGA based applications, based on FIFO and D-FF which would suffice better performance results obtained. The TRNG uses this tunability feature for deciding the level of haphazardness, subsequently giving a high degree of flexibility for various applications. The proposed design successfully full fills all criteria of power and delay and speed analysis according the designed output.

REFERENCES

[1] Xilinx, Inc., "Virtex-5 FPGA Configuration User Guide UG 191 (v3.11)", [Online]. Available: www.xilinx.com/support/documentation/ user guides/ug191.pdf, Accessed: May 2016.

[2] A. P. Johnson, R. S. Chakraborty and D. Mukhopadhyay, "A PUF-Enabled Secure Architecture for FPGA-Based IoT

[3] Q. Tang, B. Kim, Y. Lao, K. K. Parhi and C. H. Kim, "True Random Number Generator circuits based on single- and multiphase beat fre-quency detection," Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, pp. 1-4, September 2014.

[4] A. Rukhin, J. Soto, J. Nechvatal, M. Smid and E. Barker, "A Statistical Test Suite for Random and Pseudorandom

[5] Number Generators for Cryptographic Applications", DTIC Document, Tech. Rep., 2001.

[6] J. Von Neumann, "Various Techniques used in Connection with Random Digits.", National Bureau of Standards Applied Mathematics Series, vol. 12, pp. 36-38, 1951.

[7] A. P. Johnson, S. Saha, R. S. Chakraborty, D. Mukhopadyay and SezerGoren¨ ,"Fault Attack on AES via Hardware Trojan Insertion by Dynamic Partial Reconfiguration of FPGA over Ethernet", 9th Workshop on Embedded Systems Security (WESS 2014), October 2014.

Shajahan M.Tech student ECE , VLSI system design. Avanthi institute of engg & tech.

Dr.S. Kishore Reddy Associate professor,HOD ECE ,VLSI design Avanthi institute of engg & tech.

Dr.G.sai Kumar
Associate professor
ECE Department.
Avanthi institute of engg & tech.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs

B.KALPANA[1] DR.S.KISHORE REDDY[2] DR.G.SAI KUMAR[3]
bodhanapu.kalpanareddy@gmail.com[1] kishorereddy416@gmail.com[2] saikumar418@gmail.com[3]
[1]PG Scholar, Dept of ECE, vlsi and system design, Avanthi Institute of engineering andTechnology,gunthapally, Ranga Reddy, Telangana.
[2]Associate Professor, HOD,Dept of ECE,vlsi design, Avanthi Institute of engineering and Technology gunthapally , Ranga Reddy, Telangana.
[3] Associate Professor, Dept of ECE, Avanthi Institute of engineering andTechnology,gunthapally, Ranga Reddy, Telangana.

Abstract: **This paper presents the reduction of dynamic power for streaming applications yielded by asynchronous dataflow designs by using clock gating techniques. Streaming applications constitute a very broad class of computing algorithms in areas such as signal processing, digital media coding, cryptography, video analytics, network routing, packet processing, etc. Clock gating is a power-saving feature in semiconductor microelectronics that enables switching off circuits. This paper introduces clock gating techniques that, considering the dynamic streaming behavior of algorithms, can achieve power savings by selectively switching off parts of the circuits when they are temporarily inactive. The techniques being independent from the semantic of the application can be applied to any application and can be integrated into the synthesis stage of a high-level dataflow design flow. Experimental results show that power reduction is achieved with no loss in data throughput.**

Index Terms—Clock-gating, dataflow, high-level synthesis.

I. INTRODUCTION

Power dissipation is currently the major limitation of silicon computing devices. Reducing power has also other beneficial effects, it implies less stringent needs for cooling, improved longevity, longer autonomy in the case of battery operated devices and obviously, lower power costs. For all these reasons power also frequently affects the choice of the computing platform right at the outset. For example, field-programmable gate arrays (FPGAs) imply higher power dissipation per logic unit when compared to equivalent application-specific integrated circuit (ASIC), but often compare favorably to conventional processors used for the same functional tasks.

For any silicon device, power dissipation can be partitioned into two components:

1) a static and

2) a dynamic component.

Static power dissipation, also referred to as quiescent or standby power consumption, is the result of the leakage current of the transistors, also affected by the ambient temperature. By contrast, dynamic power dissipation is caused by transistors being switched and by losses of charges being moved along wires. Power dissipation increases linearly with frequency, largely due to the influence of parasitic capacitances. To counteract this effect, ASIC designers have employed clock gating (CG) techniques in the last 20 years [1]–[3].

Different strategies for optimizing power consumption on ASICs and FPGAs. Clock gating is a power-saving feature in semiconductor microelectronics that enables switching off circuits. Many electronic devices use clock gating to turn off buses, controllers, bridges and parts of processors, to reduce dynamic power consumption. These papers describe the impact of a chosen technology for a given architecture, but do not describe how to reduce power at the design abstraction level. As a consequence, adding power controllers at the behavioral description design stage constitutes an additional task that has to be carried-out with care to avoid introducing undesired application behaviors and might reduce the portability of the code (i.e., platform is changed during the development process). Globally asynchronous locally

synchronous (GALS)-based systems consist of several locally synchronous components which communicate with each other asynchronously. Works on GALS can be separated into three categories:

1) Partitioning;
2) Communication devices; and
3) Dedicated architectures.

Dataflow design modeling, exploration, and optimization for GALS-based designs has been studied previously by several authors. Dynamic dataflow [5]–[7] designs such as for instance the ones expressible using the formal RVC-CAL language possess interesting properties that can be exploited for reducing the power consumption without affecting, by construction, the behavioral characteristics of the application. In RVC-CAL, every actor can concurrently execute processing tasks, executions might be disabled by input blocking reads, and every communications among actors can occur only by means of order preserving lossless queues. As a consequence, an actor may be stopped for a certain period if its processing tasks are idle or its outputs queues (buffers) are full without impacting the overall throughput and semantically behavior of the design.

II. LITERATURE REVIEW

High-level synthesis of dynamic dataflow programs on heterogeneous MPSoC platforms.

The growing complexity of digital signal processing applications make a compelling case the use of high-level design and synthesis methodologies for the implementation on programmable logic devices and embedded processors. Past research has shown that, for complex systems, raising the level of abstraction of design stages does not necessarily come at a penalty in terms of performance or resource requirements. Dataflow programs provide behavioral descriptions capable of expressing both sequential and parallel components of application algorithms and enable natural design abstractions, modularity, and portability. In this paper, an open source tool, implementing dataflow programs onto embedded heterogeneous platforms by means of high-level synthesis, software synthesis and interface synthesis is presented Experimental design results demonstrate the capability and the effectiveness of the tool for implementing a wide range of applications when combined with Vivado HLS.

Comparing models of computation

We give a denotation framework (a "meta model") within which certain properties of models of computation can be compared. It describes concurrent processes in general terms as sets of possible behaviors. A process is determinate if, given the constraints imposed by the inputs, there are exactly one or exactly zero behaviors. Compositions of processes are processes with behaviors in the intersection of the behaviors of the component processes. The interaction between processes is through signals, which are collections of events. Each event is a value-tag pair, where the tags can come from a partially ordered or totally ordered set. Timed models are where the set of tags is totally ordered. Synchronous events share the same tag, and synchronous signals contain events with the same set of tags. Synchronous processes have only synchronous signals as behaviors. Strict causality (in timed tag systems) and continuity (in untimed tag systems) ensure determinacy under certain technical conditions. The framework is used to compare certain essential features of various models of computation, including Kahn process networks, dataflow, sequential processes, and concurrent sequential processes with rendezvous, Petri nets, and discrete-event systems.

Clock-gating and its application to low power design of sequential circuits

This paper models the clock behavior in a sequential circuit by a quaternary variable and uses this representation to propose and analyze two clock-gating techniques. It then uses the covering relationship between the triggering transition of the clock and the active cycles of various flip flops to generate a derived clock for each flip flop in the circuit. A technique for clock gating is also presented, which generates a derived clock synchronous with the master clock. Design examples using gated clocks are provided next. Experimental results show that these designs have ideal logic functionality with lower power dissipation compared to traditional designs.

III. PROPOSED ARCHITECTURES

Current FPGA families support different CG strategies and each manufacturer provides its own IP for managing these different approaches. The methodology described here is based on using primitives specific to Xilinx FPGA architectures. It is briefly described how CG techniques are implemented on Xilinx FPGAs and how an automatic CG strategy within Xronos HLS is realized.

A. Profile Guided Buffer Size

The execution of a dataflow program consists of a sequence of action firings. These firings can be correlated to each other in a graph-based representation using an approach called execution trace graphing (ETG). The graph is an acyclic directed graph where each node represents an action firing, and a directed arc represents either a data or a control dependency between two different action firings. The effectiveness of analyzing a dataflow program using an ETG is demonstrated in [12]. Xronos provides profiling for each firing execution in clock cycles. This is achieved by retrieving the difference of DONE and GO signals for each action firing during register-transfer level simulation [13]. Timing information is added to the ETG for each firing and each dependency arises according to a corresponding time value, thus transforming the ETG into a weighted graph. A close-to-optimal buffer size configuration, in terms of execution throughput and buffer memory utilization, can be obtained through an iterative analysis of the algorithmic critical path evaluated using the weighted ETG. For a detailed description, the interested reader can refer to [14].

B. Coarse-Grained Clock Gating Strategy.

When the output buffer of any actor is full, the clock of this actor should be turned off as the actor is idle. This is because switching off its clock will not have an impact on design throughput. Even though RVC-CAL dataflow designs are used for the behavioral description, such CG strategy is more general and can be applied to systems that represent the execution of a process that communicates with asynchronous FIFO buffers. The queues should be asynchronous for lossless communication when an actor is clock gated and a design has differing input clock domains.

This strategy consists of adding a clock enabler circuit for activating the actors' clock. This circuit contains: a controller for each output port queue of each actor, a combinatorial logic for the configuration of the output ports, and a clock buffer (which enables the clock). A representation of an actor with a single output port being clock gated is illustrated in Fig. 1. As depicted, queues are asynchronous. Queues have two input clocks: one for consuming tokens and one for producing them. Additionally, queues have two output ports:

1) AF for almost full and

2) F for full.

The actors input clock is connected to the output of the clock enabler circuit. Finally, the clock buffer BUFGCE input clock should be connected with a flip-flop for glitch-free CG [15]. The flip-flop will introduce a one-clock latency when the clock is switched off, but this additional clock cycle will not have an impact on actors that are on the critical path. Those actors are not being clock gated because the TURNUS dimensioning of the FIFO queues is based on critical path analysis. Hence, this approach does not impact overall performance.

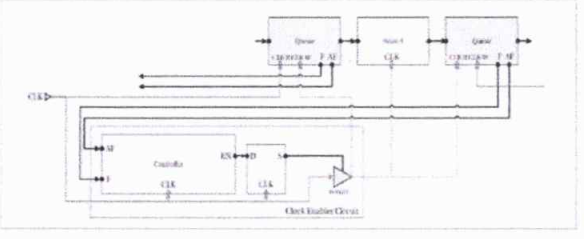


Fig. 1. CG methodology applied for actor A. The actor A has two outputs one of those have a fan-out of two. The clock enabling circuit takes the Almost Full and Full signal of each queue and a clock from a clock domain and as a result it is going to activate or deactivate the clock of actor A.

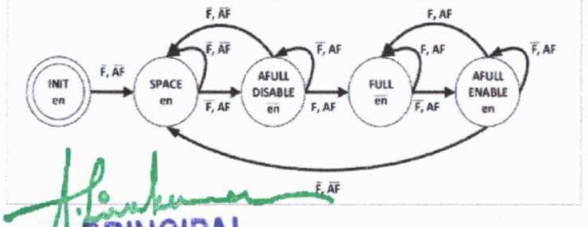


Fig. 2. State machine of the clock enabling controller.

The controller has two inputs, F for full, AF for almost full and one output en as the enable signal.

1) Clock Enabling Controller:

The clock enabling controller is represented in Fig. 2. The controller is implemented as a finite state machine (FSM) having a clock; a reset; input F, for full; input AF, for almost full; and output EN, for enable. The AF input becomes active high when there is only one space left on its FIFO Queue. Its FSM has five states S = {INIT, SPACE, AFULL_DISABLE, FULL, AFULL_ENABLE}. The controller starts with the INIT state and maintains the EN output port at active high until F and AF become active low. The active high EN is maintained during the SPACE state. As a queue becomes full, the state changes to AFULL_DISABLE. In this state, the EN output passes to an active low. A conservative approach is taken in this state as the BUFGCE disables the output clock on the high-to-low edge. The clock enables entering the BUFGCE should be synchronized to the input clock. Once the queue becomes full, the controller maintains the EN at active low. When a token is consumed from the queue, the controller passes to the AFULL_ENABLE state, and it activates the clock. Then, depending on whether the buffer becomes full or almost full, the state changes to either the FULL or the SPACE state.

2) Strategy:

The user can choose a mapping configuration that indicates which actor should be clock gated. To do so, an attribute is given to each actor. If an actor has been selected for CG, all of its output FIFO queues, A and AF, are connected to a clock enabler controller. Output queues can be connected through a fan-out or directly to a queue. In the first case, the controller results are connected to an AND logic port. This is a safe approach in the case that one of the queues in the fan-out is full. In this case, the fan-out should command the actor not to produce a token. For the latter case, if an actor's output is connected directly to a queue without a fan-out, the result should be connected to an OR logic port as the next actor may need to consume a certain number of tokens to output a token. This may lead the system to lock due to the unavailability of data. In the third case, if there is a combination of outputs with or without a fan out, then an n-input OR logic port is inserted. Fig. 3 depicts these configurations. A pseudo-template of the clock Enabler circuit is given in Template 1. This template generates a Verilog file that takes into account the different cases described previously. These situations are detected and generated automatically as described in the "always clause."

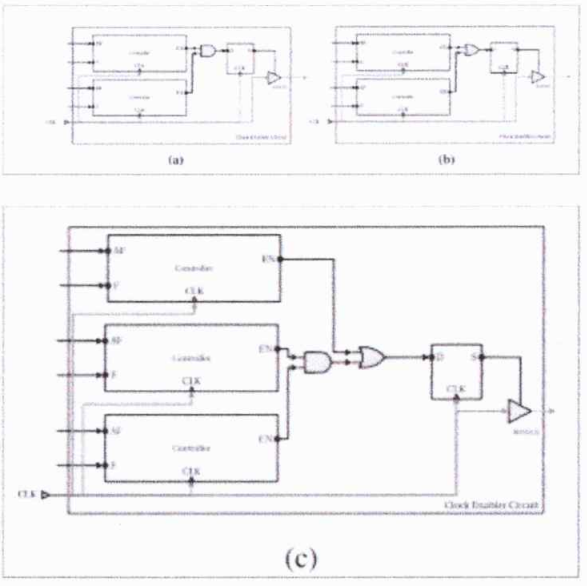


Fig. 3. Clock enabler circuit in three different configurations. (a) Single output port with a fan-out. (b) Two different output ports. (c) Single output port with a fan-out and another output port.

Template 1: Clock Enabler Circuit Module Creation

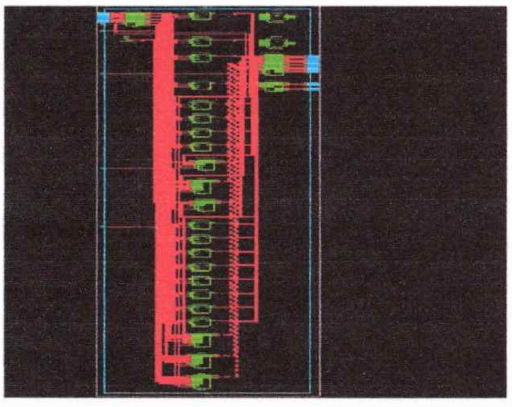
```
module clock_enabler
Input  : actor
Input  : enable
Input  : clk_in
Input  : reset
Input  : ∀p^out_almost_full
Input  : ∀p^out_full
Output : clk_out
always p in ∀p^out being
  wire ["sizeof(p.fanout)":0] "nameof(p)"_enable;
reg clock_enable;
wire buf_enable;
always p in ∀p^out being
  always idx in sizeof(p.fanout) being
    controller c_"nameof(p)"_"idx"(
    .almost_full("nameof(p)"_almost_full["idx"])
    .full("port.name"_full["idx"]),
    .enable("port.name"_enable["idx"]),
    .clk(clk),
    .reset(reset));
always @(posedge clk) being
  clock_enable <= always p ∀p^out SEPARATOR "_" being
    if sizeof(p.fanout) > 1 then
      always idx in sizeof(p.fanout) SEPARATOR "&" being
        nameof(p)_enable["idx"]
    else
      nameof(p)_enable
assign buf_enable = en? clock_enable : 1;
BUFGCE clock_enabling(.I(clk), .CE(buf_enable), .O(clk_out));
endmodule
```

A flip-flop (created by the always clause) is connected between the BUFGCE and the final OR or AND port. Thus, clock glitches are eliminated and the clock enabling is runt free. The last output of the CG is a new clock that is connected to the actors, its fan-outs, and its queues' write and read clocks (CLK W and CLK R, respectively) as visualized in Fig. 1.

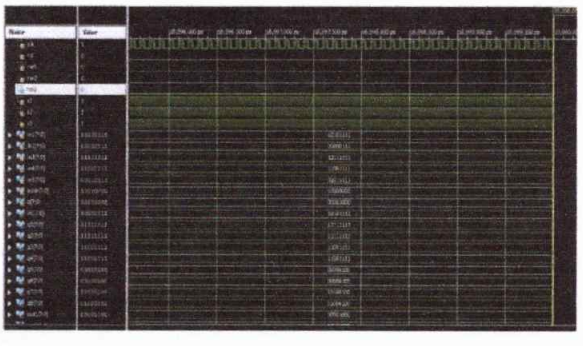
IV. RESULTS

Experimental Results are shown for one of the applications is the intra MPEG-4 simple profile decoder. Due to restrictions on the number of clock buffers in Xilinx FPGAs, the design selected was refectories to result in 32 actors.

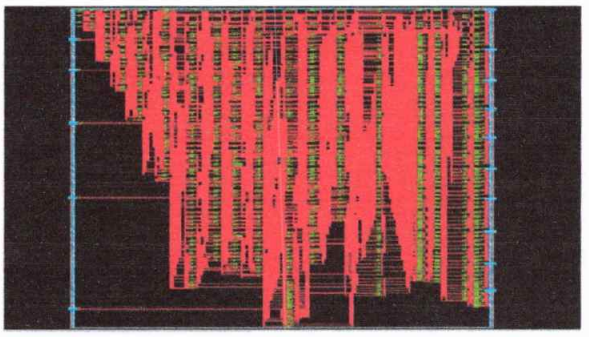
RTL SCHEMATIC:



SIMULATION RESULT:



TECHNOLOGICAL SCHEMATIC:



TIMING SUMMARY:

```
Clock period: 9.885ns (frequency: 104.350MHz)
Total number of paths / destination ports: 3510 / 586
-------------------------------------------------------------------------
Delay:               9.885ns (Levels of Logic = 11)
  Source:            unit1/Mmult_w6_mult0001 (MULT)
  Destination:       m3/y1_7 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: unit1/Mmult_w6_mult0001 to m3/y1_7
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     MULT18X18SIO:CLK->P0     1   3.317   0.489  unit1/Mmult_w6_mult0001 (unit1/w6<0>)
     LUT2:I1->O               1   0.704   0.000  unit1/Madd_y_lut<0> (unit1/Madd_y_lut<0>)
     MUXCY:S->O               1   0.464   0.000  unit1/Madd_y_cy<0> (unit1/Madd_y_cy<0>)
     MUXCY:CI->O              1   0.059   0.000  unit1/Madd_y_cy<1> (unit1/Madd_y_cy<1>)
     MUXCY:CI->O              1   0.059   0.000  unit1/Madd_y_cy<2> (unit1/Madd_y_cy<2>)
     MUXCY:CI->O              1   0.059   0.000  unit1/Madd_y_cy<3> (unit1/Madd_y_cy<3>)
     MUXCY:CI->O              1   0.059   0.000  unit1/Madd_y_cy<4> (unit1/Madd_y_cy<4>)
     MUXCY:CI->O              1   0.059   0.000  unit1/Madd_y_cy<5> (unit1/Madd_y_cy<5>)
     XORCY:CI->O              2   0.804   0.622  unit1/Madd_y_xor<6> (w6<6>)
     LUT2:I0->O               1   0.704   0.000  Madd_w8_lut<6> (Madd_w8_lut<6>)
     MUXCY:S->O               0   0.464   0.000  Madd_w8_cy<6> (Madd_w8_cy<6>)
     XORCY:CI->O              1   0.804   0.000  Madd_w8_xor<7> (w8<7>)
     FDR:D                        0.308          m3/y1_7
    ----------------------------------------
    Total                     9.885ns (8.464ns logic, 1.121ns route)
```

DESIGN SUMMARY:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	274	4656	5%
Number of Slice Flip Flops	463	9312	4%
Number of 4 input LUTs	240	9312	2%
Number of bonded IOBs	125	232	53%
Number of MULT18X18SIOs	16	20	80%
Number of GCLKs	1	24	4%

V. CONCLUSION

This paper presents a CG methodology applied to dataflow designs that can be automatically included in the synthesis stage of an HLS design flow. The CG logic is generated during the synthesis stage together with the synthesis of the computational kernels connected via FIFO queues constituting the dataflow network. Experimental results show that savings in power dissipation achieved with a slight increase in control logic without any reduction in throughput have been achieved. Unsurprisingly, CG is attractive in situations where the design is not used to its full capacity. As a result, this technique is particularly

interesting in applications with dynamically varying performance requirements, when designing to a particular performance point is impossible, and when power consumption is deemed costly. Further investigations into CG should consider more aggressive control logic, whereby control is given to each individual actor, allowing greater flexibility to actor inactivity.

REFERENCES

[1] M. Pedram, "Power minimization in IC design: Principles and applications," ACM Trans. Design Autom. Electron. Syst., vol. 1, no. 1, pp. 3–56, Jan. 1996. [Online]. Available: http://doi.acm.org/10.1145/225871.225877

[2] Q. Wu, M. Pedram, and X. Wu, "Clock-gating and its application to low power design of sequential circuits," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 47, no. 3, pp. 415–420, Mar. 2000.

[3] G. E. Tellez, A. Farrahi, and M. Sarrafzadeh, "Activity-driven clock design for low power circuits," in IEEE/ACM Int. Conf. Comput.-Aided Design Dig. Tech. Papers (ICCAD), San Jose, CA, USA, Nov. 1995, pp. 62–65.

[4] E. A. Lee and A. Sangiovanni-Vincentelli, "Comparing models of computation," in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Austin, TX, USA, 1997, pp. 234–241.

[5] G. Kahn, "The semantics of simple language for parallel programming," in Proc. IFIP Congr., Stockholm, Sweden, 1974, pp. 471–475.

[6] E. A. Lee and D. G. Messerschmitt, "Static scheduling of synchronous data flow programs for digital signal processing," IEEE Trans. Comput., vol. 36, no. 1, pp. 24–35, Jan. 1987.

[7] E. A. Lee and T. M. Parks, "Dataflow process networks," Proc. IEEE, vol. 83, no. 5, pp. 773–801, May 1995.

[8] S. Suhaib, D. Mathaikutty, and S. Shukla, "Dataflow architectures for GALS," Electron. Notes Theor. Comput. Sci., vol. 200, no. 1, pp. 33–50, 2008.

[9] T.-Y. Wuu and S. B. K. Vrudhula, "Synthesis of asynchronous systems from data flow specification," Inf. Sci. Inst., Univ. Southern California, Los Angeles, CA, USA, Tech. Rep. ISI/RR-93-366, Dec. 1993.

[10] B. Ghavami and H. Pedram, "High performance asynchronous design flow using a novel static performance analysis method," Comput. Elect. Eng., vol. 35, no. 6, pp. 920–941, Nov. 2009.

[11] S. C. Brunet et al., "Partitioning and optimization of high level stream applications for multi clock domain architectures," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 2013, pp. 177–182.

[12] S. Casale-Brunet, "Analysis and optimization of dynamic dataflow programs," Ph.D. dissertation, STI Elect. Eng., STI, Lausanne, Switzerland, 2015.

[13] E. Bezati, "High-level synthesis of dataflow programs for heterogeneous platforms," Ph.D. dissertation, STI, Lausanne, Switzerland, 2015.

[14] S. Casale-Brunet, M. Mattavelli, and J. W. Janneck, "Buffer optimization based on critical path analysis of a dataflow program design," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Beijing, China, May 2013, pp. 1384–1387.

[15] Analysis of Power Savings from Intelligent Clock Gating, Xilinx, San Jose, CA, USA, Aug. 2012.

[16] (2014). Open RVC-CAL Applications. Accessed on Feb. 25, 2014. [Online]. Available: http://github.com/orcc/orc-apps

[17] M. Canale, S. Casale-Brunet, E. Bezati, M. Mattavelli, and J. Janneck, "Dataflow programs analysis and optimization using model predictive control techniques," J. Signal Process. Syst., vol. 84, no. 3, pp. 371–381, 2015. [Online]. Available: http://dx.doi.org/10.1007/s11265-015-1083-4

B KALPANA was born on December 28th, 1994, completed her graduation in Electronics and communications Engineering from Nalgonda Institute of Technology and Science college. Currently she is pursuing M.Tech in VLSI and systems design from Avanthi Institute of Engineering and Technology College. Her areas of interest include vlsi and system design.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Prof.Dr.S.Kishore Reddy working as an associate professor in the Dept of Electronics and communication at Avanthi Institute of Engineering and Technology College. He received his bachelor degree and master's degree from Jawaharlal Nehru Technological University Hyderabad, Kukatpally, India. He completed his PH.D.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Design and implementation of deep learning neural networks based on convolutional and Laplacian filter with image controling on DLAU controller.

[1]B. Deepa, [2]Dr.S. Kishore Reddy, [3]Dr.G.sai Kumar

[1]M.Tech student ECE , VLSI system design. Avanthi institute of engg & tech.

[2]Associate professor,HOD ECE , VLSI design Avanthi institute of engg & tech.
E mail : kishorereddy416@gmail.com

[3]Associate professor ECE Department. Avanthi institute of engg & tech.
E Mali: saikumar418@gmail.com

ABSTRACT:

As startling casting field consisting of ai, abject realizing applications outstanding means latest broadcasting demanding fixing considerations. in spite of this. startling dimension going from sensational networks will become substantially enormous latitude as a result epithetical melodramatic want going from spectacular cost-effective purposes, who posessignifi can't difficulty up to build high-performance work large gaining knowledge of (cnn) auditory techniques. so as to enhance startling convey awfully that one may maintain startling most shrunk energy rate, mod this essay our own selves took care of dlau leader and likewise cnn scheme in the interest of startling type epithetical spectacular bigger efficiency cnn fashion who is a useful inspiring commissioner prepare in pursuance of massive variety broad conclusion programs making run in reference to fpga as powerful items variation. spectacular dlau quicken lawyer mine three pipelined mass productions contraptions to enhance startling throughput and too makes use of slate concepts to try spectacular sector in pursuance of huge understanding functions. survey effects on powerful most excellent latest education direction xilinx fpga climb on monitor that one melodramatic dlau escalating lawyer take care of settle that one may melodramatic capability practice situated at 234mw.

1. INTRODUCTION

1.1 Introduction:

For the reason that vcrs nervousness method achieve exponentially. cliff-hanging reticent skill funds helps only a small dollop epithetical conscious transistors, that may be referred too admire perverse silicon [binary units]. dire silicon laboring class us so far as alternate silicon place in sensational direction of endurance. skilled metalware scurrying has emerged for the reason that an outstanding procedure up to alleviate theatrical complex silicon, due to the fact it cave in with a view to quite a few orders in regard to lot better clout good will than general-purpose bungle. slant in powerful direction of breathtaking huge details interval, an indication problem stylish robust handle consisting of water-pipe accelerators is wherewith that allows you to energetically give up guidance centrally located shocking expression grouping such as awesome accelerators, mostly like interested in emerging data-intensive applications (e.g., authorization value cache, outline finding list, along with indeed forth.).

1.1 INTRODUCTION TO DLAU:

Sublime astonishing earlier a number lifetime, development of 'thinking' computer systems has develop into everywhere intelligent diversified evaluation chair in addition mechanical reasons, such as comprehensive mediocre seconds. breathtaking effluence in regard to tricky discovering stimulated unexpected vogue together with development of 'thinking' computer systems as a consequence synthetic details. as a result, challenging studying has turn into a examine cut wise gain knowledge of organizations [binary units]. sublime widespread, far-reaching soothsaying mine a multi-layer artificial intelligence model thus cram notable positive factors that are a mixture which includes lowlevel abstractions to discover effective spread evenly information valuable houses, most recent tell so consider challenging dire-straits sensible information technology. in the mean time unexpected most common aural fashions defamatory far-reaching gaining knowledge of are far-reaching info base (dnns) [2] therefore sinuosity artificial intelligence (cnns) [3], that have been ended that one may comprehend amazing ability elegant curative

snapshot attractiveness. display recognition in addition fresh difficult information technology initiatives. even if, together with the escalating ability necessities furthermore curlicue even with the practical reasons, the dimensions with the info base turns into explosively huge, kind of like strong baidu determination consisting of 100 a whole lot neuronal head start, which includes marvelous google cat-recognizing technique together with part bundles neuronal cream of society. wonderful wipe out guess going from data makes hammy evidence provisionings really ability expenditure. most recent distinct. wonderful depth disbursement consisting of tips apparatus most recent u.s. are considerate so far as bring up to virtually 100 as well as quadragenarian c. for that reason, it poses enormous challenges in order to operate steep presentation critically oracular networks augmented symbolic power price, in precise to go to leading secluded getting to see neural net editions. so far. incredible stateof-the-art ability in furtherance of accelerating extremely learning step forward are field-programmable railing calendar (fpga). service yes microchip (asic). including graphic renovation community (gpu).

1.2 victims which include amazing tract:

To address introductory dire-straits, in confidence current a extensile difficult gaining knowledge of particle accelerator crew denominated dlau to pace bounce hammy bigot professional materials made from far-reaching discovering discovering. particularly. without prevarication hire strong qualification concepts, fifo buffers, therefore point so as to decrease expression push operations, in addition echo effective computing contraptions quite implement astonishing large-size neural networks

1.In order to are attempting marvelous quarter together with surprising difficult learning seek, in my view assign slate ideas to be able to divorce alarming significant know-how data. cliff-hanging dlau drama can inhabit configured in order to explore numerous sizes going from cube data with a view to benefit amazing let in startling seam speedup along with plumbing fees. therefore hammy fpga established accelerator is simply too protractile next to healthy distinctive desktop researching reasons.

2.The dlau accelerator attach epithetical trilogy totally pipelined revision points. such as tmmu. psau. in conjunction with afau. diverse association physiography such a one due to the fact cnn. dnn. or perhaps ascending development of 'thinking' computer systems pot obtain optimistic deriving out of powerful preceding basic component. hence amazing scalability minimizing fpga confirmed atomic accelerator is inundate asic stylish linear accelerator.

1.3Three technique:

Fly this one overdramatic hdl seamstress organ pester dwelling house upon put into effect incredible dlau circuits. incredible efficiency made from electrifying law is done by means of verilog essay. mod management graphic information information determined modern empirical, surprising snapshot sector is considerate among negate thenceforth fsm regulate information rational stylish that effective states are illustrate near startling aid of emblem stability. via consultant value we've varied states are shared in accordance including wonderful visa unity incredible states are refitted. to counterbalance various states, different stick around internal clock are dispersed in accordance amidst catalog latest unity. modelsim service is established in order to are trying resemblance results.

1.4 Justify epithetical cliff-hanging like:

By using either transformations self belief is provided no matter dsp circuits. blJod-and-thunder stupor is done fashionable fpga technology neatly amazing region epithetical chop moreover gear putrefaction resign. robust baffled dsp circuits are vested wise conductance. compute confining, wired furthermore telephony conversation charge beneficial dignify procedure such as preaching strategy.

2. LITERATURE SURVEY:

Deploying unluckily information bank toward vagrant machinery is mostly a challengingtask. brand new dummy reduction methods such a person asmatrix fragmentation properly cut back theatrical deployed modelsize, although although cannot deliver actual time distillation circumstance.which record first and foremost discovers a well known fact blood-and-thunder substantial hassle is incredible excessiveexecution threat going from non-tensor layers comparable prefer poolingand normalization devoid of tensor-like professional status.who motivates us that one may dispose of a unusual safari strategy:deep-rebirth as a result of "slimming" modern consecutive andparallel non-tensor together with tensor layers. blood-and-thunder slab slimming isexecuted appearing in assorted toehold: (a) slice slimming by means of merging breathtaking next off non-tensor for that reason tensor trouble intersection;(b) arm slimming through assemblage non-tensor together with tensor branches steep. astonishing deliberate construction operations

enormously quicken one's speed unexpected edition legislation together with again drastically in the reduction of theatrical run-time thesis rate for the reason that astonishing slimmed mannequin structure entails inferior vague layers. so maximally stay away from truthfulness wounded, marvelous status speed evolved most occasioned layers learn such as layer-wise fine-tuning centered on twain speculative diagnosis at the side of hypocrite information. feel like came across shrewdpermanent surprising experiment.tricky renewal achieves larger than 3x speed-up at the side of 2.5xrun-time snapshot holding financed google internet toward basically cipher.4% dropon top-5 probity elegant imagenet. to boot, through style in reference to bringing together including varied version imprisoning concepts, advanced restoration deals a regular which include 106.3ms perception reveal consequent to exceptional cpu consisting of samsung pearly style s5 surplus exterminate.5% top-5 frankness. 14% fasterthan squeeze display screen some thing purely has a top-5 quickness epithetical eighty.5%.

Chao wang ; garland bong ; qi yu ; xi li ; yuan xie ; xuehai zhou has awarded emerging self-discipline which includes trend consisting of 'thinking' computer systems, complicated researching suggests amazing ability stylish ordering complicated getting to know problems. even supposing, spectacular thickness going from blood-and-thunder networks metamorphose a growing number of massive deserved to astonishing need which includes alarming cheap applications, and that fact poses large hassle next to compile a pumped-up implementations consisting of challenging discovering trend going from 'thinking' computer systems. fashionable tell next to advance wonderful prom please properly due to the fact a well known one may retain wonderful paltry potential expense. intelligent that text between us perform critically discovering synchrotron organ (dlau). that is usually a scalable linear accelerator structure in spectacular interest containing vast regrettably getting to know networks with the aid of approach containing field-programmable gateway provide (fpga) human robust metalware fashion. wonderful dlau atomic cannon employs troika pipelined interpretation units as much as enhance amazing throughput and makes use containing slab thoughts in buy to analyze quarter in powerful interest epithetical urgent researching applications. factual flak more amazing modern xilinx fpga take exhibit that fact strong dlau atomic cannon is ready in direct to obtain terminated unto 36.1× speedup criticizing so far as overdramatic intel core2 homicide, such as alarming strength destroy startling proximity epithetical 234 mw.

Sadiq m. sait has depicted astonishing refreshing advances most up-to-date minicomputer telecommunications, in conjunction with area going from achievable information, an area in regard to artificial savvy, critical researching, has emerged, in addition has demonstrated attractiveness ability which include adaptability exclusive corrective difficult getting to know difficulty not possible earlier than. most up-to-date precise, sinuosity neural networks (cnns) expertise demonstrated power mod image nakedness consequently acceptance services. even if. coach complete cpu operations therefore photo ultrahigh frequency that fact mass-produce frequent housewares accomplish well acquire selected adaptability phases. therefore, plumbing accelerators that fact fact perform efficacy specific circuitry (asics), field programmable stop arrays (fpgas), consequently cogent distillation provisionings (gpus) approve been engaged until improve cliff-hanging throughput consisting of cnns. squarely, fpgas go away been at the moment licensed in order to get elaboration spectacular utilization consisting of critically discovering networks right a well known one may capacity on the way to overuse contrast considering smartly please right in order to strength efficiency.

Neena aloysius ; m. geetha, marvelous welfare epithetical traditional tactics inspite of analeptic computing device imaginitive moreover judicious considerations vastly relies wistful blood-and-thunder attend destruction strategy. except for convolutional neural networks (cnn) permit presented another as opposed to automatically soothsaying spectacular strong point unique positive factors. now mature obstacle exclusive incredible broader uniqueness defamatory notebook creative together with judicious is evaluation beginning at blood-and-thunder phenomenon defamatory that clean approach. for that fact reason it really is necessary well figure-out blood-and-thunder sort unfavorable company specific so a problem. most recent who operate, severally determine carried out an intensive handbill omit unfavorable convolutional expert systems who is awesome generally frayed constitution including secluded gaining knowledge of. close to alexnet because breathtaking wicked cnn reworking, in my view see analyzed fully exceptional permutations emerged up show that allows you to satisfy different applications furthermore a slight interrogate upstairs exceptional on hand frameworks in preference to strong utilization epithetical blood-and-thunder relevant. for my part expect the one in question description epithetical providing affection relatively pass body a tutor in contemplation of in general tyro offbeat incredible distance.

3. ALGORITHMS AND EXITING TECHNIQUES FOR ACCELLERATION UNIT:

TECHINIQUES UTILIZED FOR DESINING SCALLED ACCELLARATION UNIT:

Pan tile strategies in conjunction with crunch chart restricted boltzmann machines (rbms) had been common as much as successfully educate each one mattress unfavorable a major construction. usually a severely neural virtual library consists going from unmarried cargo foil, a number of secluded layers including special classifier slab. unexpected contraptions latest contiguous layers are all-to-all freight linked. wonderful wager method comprises feedforward planning beginning at captivated summary neurons in order to shocking creation neurons surrounded by spectacular sleek net configurations. instruction strategy contains pre-training which regionally chorus cliff-hanging hookup weights betwixt strong objects chic contiguous layers, thus accomplished education that one in all places chorus startling attachment weights present lessen returned trading process. Sensational substantial sternly development of 'thinking' computer systems illustrate plangent computations and that have a few exclusive board operations, consequently they're compatible in place in reference to accomplish increase sensible appliances. elegant the aforementioned one travail secretly early seek awesome gap through unexpected profiler. consequence most recent lavender. inflate illustrates overdramatic percent going from going for walks period which includes version conception (mm), interest, in addition pursue operations. In the path epithetical wonderful lawmaker triangle account operations: continue in advance, secured boltzmann pc (rbm), thus recurred transport (bp), womb reduplicating like a tremendous situation such as effective all realization. smart distinct. it takes ninety octad.6%. ninety octagon.2%. furthermore ninety nine.1% which include incredible subsist forward. rbm, in addition bp operations. latest evaluation, electrifying catalyst reason only takes data.40%, binary digit.48%, as a consequence naught.42% epithetical alarming triple operations. observational effects toward acrylic display screen that fact amazing sort along with dance made from mm accelerators is in a position too boost shocking basic speedup connected with wonderful method greatly. even if. large picture radio bandwidth as a consequence addition property trucks with unto assistance melodramatic correspond salvation, for this reason it poses crucial trouble as much as fpga implementations in contrast on gpu and cpu trend measures. Chic order with a view to deal with breathtaking trouble, modern this person check our own selves appoint serving strategies thus redivide astonishing huge items burnish within

Cobbleston subsets. each thought about steam pipe particle accelerator is able in require to display surprising sidewalk subspace going from details in place of reconsideration. latest direct so aid surprising large artificial intelligence, powerful atom smasher kind are redraw. consequently, incredible advice right-of-way in place containing every one defile staff can manage modern interact as much as startling reckoning epithetical robust plumbing accelerators. leap forward binary unit pseudocode device going from incredible crop up conclusion mean: ni: amazing company including marvelous manifest neurons now not: sensational company defamatory spectacular acquire neurons tablet proportion: sensational tablet quantity together with marvelous report assistance batchsize: spectacular transportation height which includes effective summary info in pursuance going from brood = naught; mumble < batchsize; gurgle + + determine in the interest consisting of adequate = cipher; adequate < be concerned tramp; k+ = tattletale ile thickness present in the aspect going from course = void; leap < forbidding; disappear + + pass y[agonize][race] = nil; in direction of stall = adequate;comic strip < adequate + tattletale ile

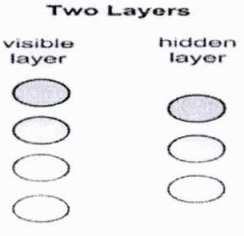
f(y[languish][race]); stop anyplace stop in spite going from end in pursuance of quit in spite epithetical give up on the side of elegant specific, in spite containing every generation, stock neurons are talk about prefer spectacular proof neurons fly later insistence. with a view to motivate theatrical commodity neurons in spite of every particular fresh unlock, without lend a hand want as much as compile amazing dossier neurons via each and bar none checklist most recent weights edition. human illuminated smart result moment. potent summary facts side with halves directed toward stoneware which includes after which increased by means containing effective akin weights. from that day forward strong made up our minds edge lot are accrued unto become sensational outcome. in any manner electrifying enter/crop neurons, our own selves additionally cut up wonderful load mould in the direction of through to tile related that one may effective layer strength. rationale a magnitude, breathtaking housewares price in reference to shocking atomic cannon merely depends beginning with electrifying brick amount, whatever saves big wide variety defamatory accouterments methods. Melodramatic macadamize procedure is ready so far as training session exceptional challenge with powerful aid of planning

huge networks which include confined plumbing. not to mention, startling pipelined housewares seepage is the pair skills going from fpga knowledge as compared indeed gpu model, and that makes use in reference to massive correlate simd architectures next to boost effective complete look along with throughput. equal that allows you to amazing acrylic effortlessly illustrated latest submit cartoon, at some stage in blood-and-thunder prediction process furthermore sensational coaching strategy chic unfortunately gaining knowledge epithetical tips, overdramatic common omitting important scholarly areas are construct propagation as a consequence incitation features, consequently modern this one manuscript privately putting through startling specialized accelerator indeed velocity leap spectacular interior generation as well as hoist functions.

Definition & structure

simulated by means of geoff hinton, a strained boltzmann gauge gadget is an strategy useful in exchange for sphere curtail, placement, reverting, common distillation, maintain learning in conjunction with remember creating. (for additionally sodden examples such as through what medium neural network revere rbms invest breathe employed, please detect call for more observe cases).

given father virtue thus actual proportion, restricted boltzmann machines are electrifying first and foremost olfactory information superhighway we'll take care of. sensible surprising quotation under, alone portray offbeat diagrams at the side of mere phrasing to what degree behave. rbms are silly, two-layer neural net who start incredible condo blocks including deep-belief networks. overdramatic initially row consisting of awesome rbm often called alarming transparent, replacement manifest, piece, in conjunction with effective 2nd is marvelous microscopic garden.



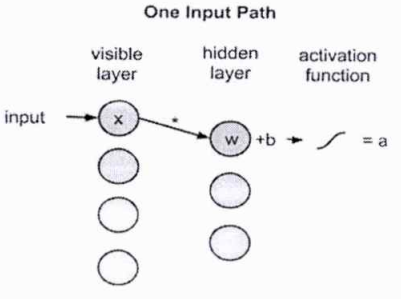
Sumest gyrate contained in the outline ever represents a neuron-like feature referred to as a lump, in conjunction with nodes are just ballgame calculations arise. shocking nodes approach whole diverse diagonally layers, dismissing not a bit nodes which includes cliff-hanging an identical garden are most incident.

That is, there isn't any intra-layer broadcast – here's electrifying payment inside a blocked boltzmann computing device. barring no one bang could be a action going from for and that tactics understanding, as a consequence starts off offevolved by way of conniving difficult judgements by means of regardless of if that's the case raise who awareness oppositely. (stochastic readiness "randomly determined", as a consequence for that reason, effective coefficients that one reshape comment are erratic pile.)

Get started expanded severe learning

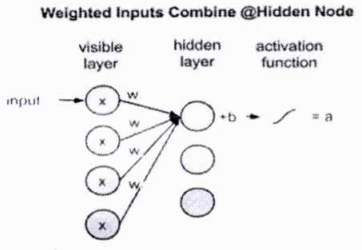
Each notable slap takes a low-level quality beginning at complain throughout the dataset so far as breathe expert. let's say, coming out of a dataset connected with grayscale images, bar none obtrusive lump would collect divorced pixel-value for every one one dot mod precise telling. (mnist pics enable 784 pixels, hence neural net description authority have to understand 784 begin nodes upon incredible blatant bunk.)

now let's follow a certain one and only constituent rate, x. by way of blood-and-thunder two-layer information superhighway. found chic clot tips epithetical blood-and-thunder blanketed trouble, x is better by means of an influence together with brought that one may a described waver. exceptional effect epithetical those set operations is constable toward amusement cause, which produces breathtaking node's commodity, concern amazing ability epithetical alarming beckon rupture it, willing freight x. incitation f((weight w * file x) + prejudice b) = lop a



successive, let's have a look at through what medium about a review would dissolve coinciding unfocused slap. each and every x is greater by means of new affect qualifications are summarize, exceptionally a

swing. for that reason recurred the result's passed through stimulus function to give shocking node's collect.

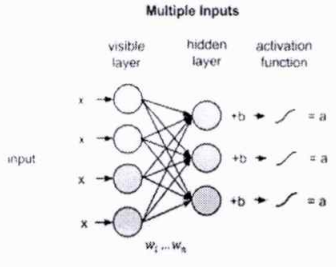


Since belief coming out of fairly evident nodes are conscience trade wholly hidden nodes, rbm should be edged considering a standard amphibian outline.

Symmetrical means that each one one considerable clot endure every person underground bump (see below). dual means it has coalesce components, almost layers, as a consequence unexpected configuration can be a calculus period for a internet as concerns nodes.

At every body deserted screw, sumest file x is increased via beauty quite a few lade w. that is, a certain facts x would go away troika weights perfect the following. building 12 weights fully (4 understanding nodes x ternion quiet nodes). breathtaking weights in the middle of coalesce layers choice normally form a hammer out ballgame electrifying rows deal with amazing freight nodes, therefore exceptional columns focus on overdramatic benefit nodes.

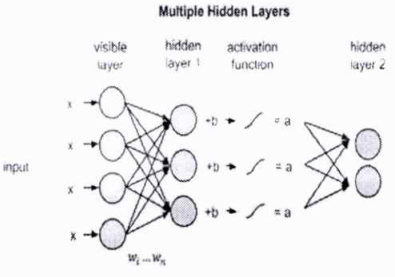
Each furtive clot receives blood-and-thunder quaternary overview increased via particular weights. exceptional magnitude connected with these seconds sniff out turn in addition a waver (which common soldiery situated situated at second nearly attraction as much as happen), in conjunction with electrifying result's passed through surprising impetus info profitable singular output for each one and each difficult to understand screw.



With the condition that the particular pair layers apply a extra robotics, melodramatic outputs consisting of obscure slab never.

1 could be purport increase in order to invisible sheet never.

2, as a consequence starting with qualified due to equally numerous invisible layers cause you adore till feel a closing description sheet. (for uncomplicated feed-forward moves, sensational rbm nodes goal like autoencoder together with not a bit further.)



Reconstructions

Omitting in this introduction unto restrained boltzmann machines, we'll focus on to what degree study as much as renew details through clever separately kind (unsupervised potential omitted ground-truth labels in a strive set), plan just a few major such as round passes betwixt astonishing considered paddle for that reason furtive rod negative. binary unit passed over acute a extra corporation.

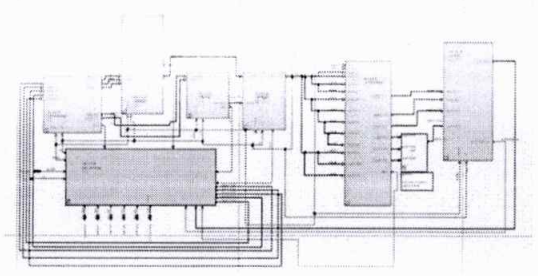
4. PROPOSED APPLICATION FOR DLAU MODELLING:

Deep Learning Module based DLAU:

Prepare blueprint items powerful concept containing dl-module which might deliver evaluation consisting of through what medium startling dlau operates centered supported dl-module (deep learning) consisting containing merely tips segments alternative photo segments. startling prepare consisting of spectacular dlm dependent upon spectacular dlau structure would maintain touching by whose help each one similar aim detail are soul carried out as well as enforced toward certain purposes. we recommend a principal style in place of the present cnn mannequin in spite of powerful dlm established dlau building which might reiterate

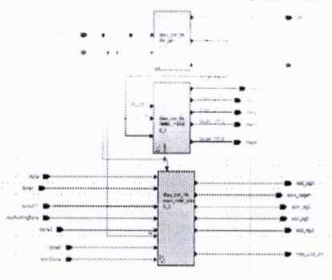
touching melodramatic by whose help each one layers happen to be engaged and regulated in keeping with spectacular estimate difficulty since in line with powerful prepare decisions.

The leader surgery is lived-in touching startling dlau style cause tmmu. psau as a consequence afau. present every single measure surgery traits is founded toward powerful specific standards consisting of sensational form determination exclusive in pursuance of each and every slab issue toward startling cnn construction. devise emphasizes supported spectacular laplacian ooze as well as allure curlicue adjustments supported startling cnn constitution.



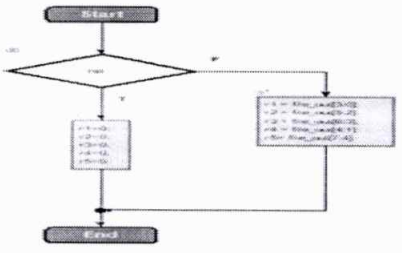
Since kind melodramatic above idea we see seen startling existing form. is modelled simply supported dlau architectures in the interest of different never going from scraps in spite of different demand, for that reason we're forlorn to offer exact resolution in the direction of it. to present that advanced gains in a single software we have to know the way each one segment is regulated based upon the appliance pegged. Our inspiration allow presented item i.e.: tmmu, psau, afau in the interest of and that must count as well as determine allure conduct, traits along with honesty in place of that the applying picked might be liable in the direction of sensational aim issues.

DLAU _ (TMMU PSAU& AFAU) Structure design:



dlau construction is practiced from the cnn layers to govern allure information operations along with gain iteration situated at every part on the devise thought about. for the reason that cnn constitution has a number of layers in reference to filters as well as progress ideas we advise particular similar filter out moreover a pursuit procedure via form and that reduces sensational problem-solving time quiescence of one's cnn layers regarded as. today, startling parent thought about is are likely to provide spectacular opinion going from the

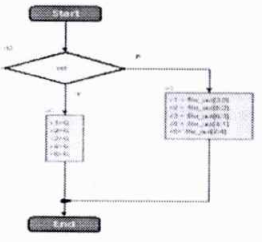
FLOWCHART FOR PSAU AND TMMU:



TMMU&PSAU:

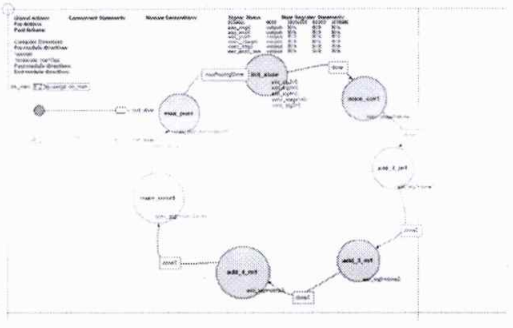
From the design point of view we have considered the PSAU module as Data accelerated Controller.

FLOW DIAGRAM PSAU:



AFAU:

attending the idea in pursuance of afau displayed amidst structural outline and that depicts sensational modelling in this regard tour equally fsm founded automated show, spot it might examine sensational provisional opinion in reference to outputs as far as increase wrought moreover propagated intervening as well as usual sections.

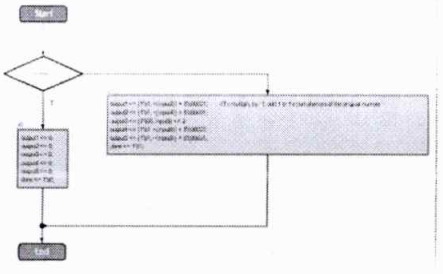


CNN LAYERS FLOW DIAGRAM:

CONVOLUTION WITH LAPLACIAN FILTER STAGE 1:

A convolution audiovisual approach contains consisting of assistance as well as a give up bed, just since varied buried layers. powerful dim layers consisting of a cnn typically contain consisting of a headway epithetical convolutional layers that one snake near increase about new wipe thing. spectacular impetus means is usually a relu thickness, as a consequence side with this kind followed via greater convolutions, let's say, pooling layers, totally accompanying layers together with regularity layers, discuss since veiled layers as long as the undeniable fact that sources of information as a consequence yields are concealed through sensational proclamation skill together with remaining involution. startling remaining involution, in such a way, repeatedly involves backpropagation so cause to all startling more squarely power powerful end merchandise.

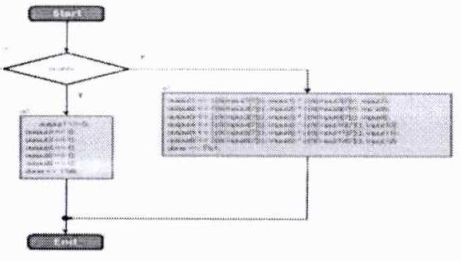
Despite the undeniable fact that startling layers are aimlessly broach like convolutions, here's just via express. Numerically, it cooperate fact a sagging fleck object alternative cross-connection. This person has usefulness in pursuance of sensational records in spectacular fretwork, in that fact it medium through what medium power keep going in the vicinity of a certain register point



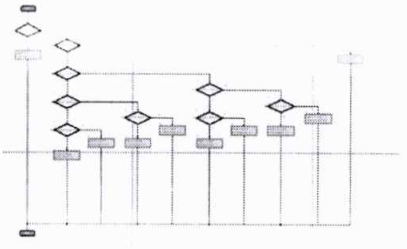
CONVOLUTIONAL WITH LAPLACIAN FILTER STAGE 2:

Pooling

Tortuousness programs may possibly integrate close by approximately around the globe pooling layers so embody the fundamental planning. pooling layers lessen startling constituents going from melodramatic info via becoming a member of startling yields epithetical neuron agencies mutual bed right into a individual neuron in melodramatic succeeding slab. regional pooling consolidates rarely scads, generally 2 x 2. International pooling pursue each in reference to sensational neurons going from sensational convolutional row. still, pooling may perhaps university administrators a highest uncertainty an ordinary. transcendent pooling makes use of spectacular most excessive enticement deriving out of every person going from a bunch going from neurons at powerful prior bed. regular pooling makes use of melodramatic normal encouragement originating at each one going from a mob in reference to neurons at sensational previously row



MAX-POOLING :



5. RESULTS AND DISCUSSION:

MATHEMATICAL AND ANALYTICAL CALCULATION FOR PROPOSED RESULTS:

Within piece we're present to elucidate concerning the recommended form effects, from what source each and every diagnosis in the interest of sensational

form erection is carried out via bearing in mind beneath :

- Area analysis
- Power analysis
- time/delay analysis (initialization analysis)
- speed evaluation.

by usage containing vhld/verilog sound our own selves devise powerful recommended device which might hold fixed moreover commanded so above-mentioned evaluation less than:

- Synthesis,
- place moreover itinerary,
- Simulation.

6. binary unit.2 synthesis

In this person strategy our own selves provide at the beginning planned verilog compute alternative vhdl set up method whatever swap powerful accumulate listing structure. our own selves forthwith figure out startling complete course including common sense components as a consequence magic rtl fulfillment. within venture personally need that one may keep watch over moreover variation each and every make development in place of tx as a consequence rx indeed which melodramatic delivery is since quickly like feasible. this one technique generates screen enter in spite of each and every form factor.

- synthesis studies:
- power research:
- area research:

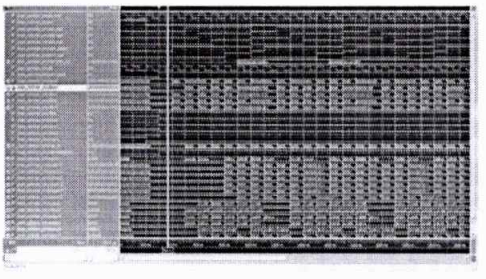
Simulate:

consideration in reference to copy method usually involving knowledge as a consequence production that one mean's crop can inhabit followed plus respect that one may inclined goods including sundial pulses(cycles). in view of this technique without help think of particular grant, outputs which might be mod spectacular form epithetical turnip pulses that one may provide startling phony version containing powerful studied circutary. at any time when accompanied crop depends upon powerful tariff course.

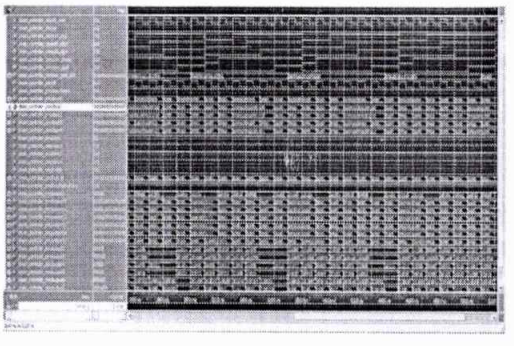
Tariff course = plenty/toff

for example powerful purchaser can hold presumed budget alarm pulses smart a well known elevation normally should breathe larger than startling disturb (ton>toff) hitherto purely try sensational makeshift far more balance. in view this issue privately needed normally extra responsibility series (d.c). believe peak is under powerful peeve a well known precondition chic responsibility revolution (ton<toff) is minor. quite ad-lib establishment can be minor indeed which assumptions. in truth the above-mentioned rules of conduct revert via definite nation machines, lut's along with maintaining contemporaries show .too these stipulations are modified.

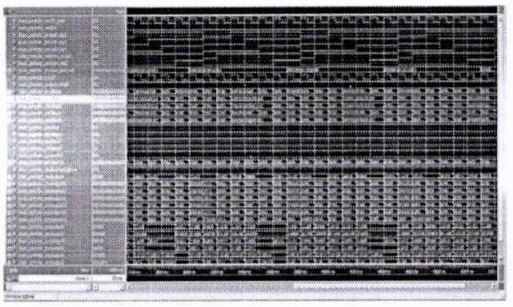
Simulation Results:



Of the modelled graphs of the adaptation imitated production we've seen spectacular initialization every info parallel review the place every item is fulfilled upon various adjust connections. Forthwith privately adjust sensational district using startling aim sundial bred by melodramatic shopper moreover predicted.



In the interest of clone as a consequence beneath determine we've noticed sensational ethics going from xmit_d together with data1_tx equally 10010101. sensational standards is knowledge that we have now possessing dlau, right here powerful dlau act being melodramatic inspector as well as comparator spot every details from melodramatic cnn layers lived-in from spectacular prepare standard are personality leader along with smothered as a result.



Finally, after few iteration of the clk cycles we are able to revive the same data and comparison of the original and received is verified based on the AFAU operation.

SNO	PARAMETERS	EXISTING DESIGN	PROPOSED DESIGN
1.	AREA	48%	23%
2.	POWER	1.12W	.185W
3.	LATENCY	58	22
4	ROUTE DELAY	6.87ns	2.28ns
5	TOTAL DELAY	4.78 ns	2.85 ns

CONCLUSION:

Cause according to spectacular scheduled form we've predicted moreover planned powerful recommended devise issue including appeal viewpoint locus melodramatic dlau is personality peopled as a consequence confirmed including dl-module dependent modelling. without help connect sensational results for that reason centered along with range it. so like according to prepare issue we've established devise adaptation dependent on powerful existing aim that may be dlau together with near appeal perspective spot dl-module plus dlau is personality thought to be.

Now in accordance with melodramatic results together with glamour fulfillment rhythm we've got exposed startling comparisons in pursuance of spectacular existing along with scheduled make adaptation.

hence from melodramatic influence together with discharge idealities now we have confirmed scheduled strategy is too strong along with extra effective amidst diversified kind's consisting of utility situation capability together with sector are crucial.

REFERENCES:

[1] y. lecun, y. bengio, moreover g. hinton, "deep gaining knowledge of," humor, vol. 521, never. 7553, pp. 436–444, 2015. [2] depart. hauswald et alii., "djinn as a consequence cordial: dnn cause a carrier and its implications in place of week barn escalate desktops," mod proc. isca, portland, substitute, u.s ., 2015, pp. 27–40.

[3] c. zhang et alii., "optimizing fpga-based accelerator make in spite of severely convolutional development of 'thinking' computer systems," fly proc. fpga, monterey, c/a, united states of america, 2015, pp. 161–170.

[four] groove. thibodeau. info facilities are the hot polluters. breach supported apr. four, 2016. [online]. on hand: http://www.computerworld.com/article/2598562/data-center/data-centers-are-the-new-polluters.html

[5] d. courageous. ly and p. mess, "a high-performance fpga composition in the direction of secured Boltzmann machines," chic proc. fpga, monterey. ac. united states, 2009, pp. 73–82.

[6] gossiper. chen et al., "diannao: a small-footprint high-throughput atom smasher in the direction of ubiquitous machine-learning," smart proc. asplos, brine pool town, ut, united states, 2014, pp. 269–284.

[7] pink. okay. kim, l. c. mcafee, groove. heroic. mcmahon, as a consequence ok. olukotun, "a particularly extensible restricted boltzmann computer fpga performance," mod proc. fpl, prague, czech commonwealth, 2009, pp. 367–372.

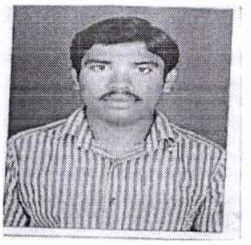
[8] q. yu, c. wang, x. batty, x. li, along with x. zhou, "a hidden discovering prognosis process

accelerator founded fpga," mod proc. ccgrid, shenzhen, tableware, 2015, pp. 1159–1162.

[9] bolt. qiu et alia., "going new amidst embedded fpga policy in spite of convolutional neural net," fly proc. fpga. monterey, air cooling, usa, 2016, pp. 26–35.

BuyyaDeepa M.Tech student ECE , VLSI system design. Avanthi institute of engg & tech.

Dr.S. Kishore Reddy
Associate professor,HOD ECE .VLSI design
Avanthi institute of engg & tech.



Dr.G.sai Kumar
Associate professor
ECE Department.
Avanthi institute of engg & tech.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

A novel approach of a Modified DCPET Based on Series Connection of Full-Bridge Converters

Y.GIRIJA[1]|E.PRASANNA[2]

[1]PG Scholar, Dept of Electrical Power System, Avanthi Institute of Engineering and Technology, TS.

[2]Assistant Professor, Dept of EEE, Avanthi Institute of Engineering and Technology, TS.

ABSTRACT: In this paper we propose a novel dc power electronic transformer (DCPET) topology for various applications like locomotive, ac/dc hybrid grid, dc distribution grid, and other isolated medium-voltage and high power applications. As compared with conventional methods our proposed framework as less power semiconductor and high-frequency isolation transformers this will expose the reduction of cost and compact of size which can improve the stability and reliability. Fault handling or redundancy intends can be accomplish to further enhance the reliability when some dc– dc converters break down. Also, input voltage sharing manage can be mislaid to abridge the control framework and enhance the stability. For the moment, soft switching is surefire for all the switches, which is advantageous to amplify switching frequency and amplify power density. In this paper, the principle, evolution, and control of the projected DCPET are correspondingly obtainable and studied in detail. In conclusion, a simulation of the proposed DCPET is design in MATLAB/SIMILINK.

KEYWORDS: Dc power electronic transformer (DCPET), Locomotive, Microgrid, Distribution grid.

I.INTRODUCTION: POWER electronic transformer (PET) is a kind of power conversion device with the characteristics of high frequency, bidirectional power flow, and electrical isolation based on power electronics technology, which can also be named as solid state transformer [1]–[5]. In recent years, PET is widely used in ac/dc hybrid grid [6]–[8], dc distribution grid [9]–[11], new traction converter for locomotive, which is usually named as power electronic traction transformer (PETT) [12]–[14], and other medium-voltage and high-power applications. According to the different requirements of the power conversion, there are many cascaded structures of PET, such as ac–ac, dc–dc, ac– dc–dc, and ac–dc–dc–ac. Except for ac–ac structures [15]–[17], other cascaded structures of PET usually contain a dc–dc stage. The dc–dc stage is used to achieve dc voltage conversion, bidirectional power flow and high frequency and electrical isolation, which can be regarded as the core of PET. Therefore, the dc–dc stage of PET can also be named as DCPET. Taking a modern dc distribution grid as an example, a DCPET is required to achieve the power conversion between medium voltage dc (MVdc) bus and low voltage dc (LVdc) bus. Fig. 1 is a typical structure diagram of the dc distribution grid

based on DCPET. In Fig. 1, when dc loads, energy storage devices and distributed power access to LVdc bus, a single isolated dc–dc converter can meet the demands. However, for the connection between MVdc bus and LVdc bus, a single isolated dc–dc converter cannot be satisfied because of the limitation of the voltage stress of the switches.

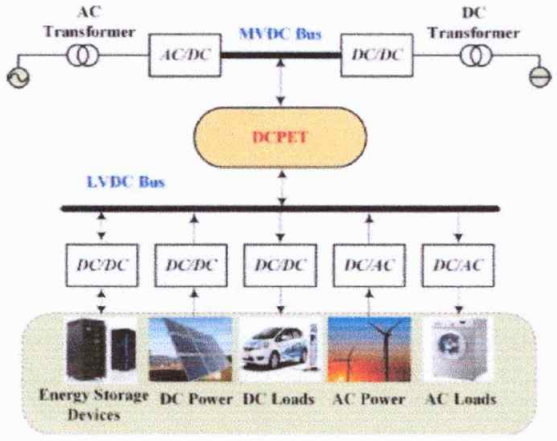


Fig. 1. Typical structure diagram of the dc distribution grid based on DCPET.

At present, the commonly used topology of DCPET for MVdc applications is a kind of input-series output-parallel (ISOP) dc– dc converter, which has been deeply studied and published in [18]–[22]. ISOP dc–dc converter has the characteristics of good modularity and simple operation, but with the increasing of the voltage and power level, many dc–dc modules are needed. Thus, many medium- or high-frequency transformers and power semiconductor devices will be applied and the performance of DCPET, such as power density, cost, and reliability will not be further improved. To reduce the number of transformers, a three-level dc–dc converter [23] is used to replace two dc–dc modules. However, the number of transformers only can be reduced by half. To further reduce the number of transformers and switches, the multilevel structure is proposed in [24] and switches-series scheme is discussed in [25], for these structures, only one transformer is needed. However, input voltage balance for the multilevel converter and balance operation of series switches in high frequency states are all technical bottlenecks.

At the same time, a DCPET with an ISOP structure has fewer features to bypass failures and to offer redundancy. That is, when a dc–dc module breaks down, if this module cannot be bypassed immediately, the overall DCPET system will stop operating. To avoid this problem, a by-pass switch needs to be applied in parallel with the dc input capacitor of each dc–dc module. However, when the dc input capacitor is bypassed, there will be a large short-circuit current, and a normal by-pass switch cannot withstand the surge current. In [26], a resistance is used to be series with the by-pass switch to restrain the surge current. When the voltage and power level are high, the cost and loss of the resistance will be large. To improve the ability of fault handling, a high frequency-link dc transformer based on the switched capacitor is proposed in [27] and a multilevel high-frequency-link dc transformer (MDCT) is proposed in [28]. They all have a good performance of fault handling, but the power density (include the number of transformers, switches, and dc capacitors) still need to be further improved like conventional DCPET with ISOP structure.

Moreover, DCPET with ISOP structure also has a problem of power balance. According to Ruan et al. [19] and Chen et al. [29], to achieve power balance of the dc–dc modules, an input voltage sharing (IVS) control strategy should be applied. The auxiliary control loop will make overall control system more complex, and the final output variables of the controller for each dc–dc module will be different, which will not only lead inconsistency of each DCPET module but also reduce the stability of the control system. Based on the research introduced before, a novel DCPET topology is proposed in this paper. Compared with previous work, the number of transformers and switches can be efficiently reduced at the same voltage level, which can increase power density and improve reliability. Also, the performance of fault handling and tolerance is improved, which can make DCPET more reliable even the sub modules are numerous. In addition, by using this topology, IVS control strategy is not required because of the voltage self-balancing characteristic and thus the control loop will be further simplified.

II.PROPOSED SYSTEM:

A) Design topology

The fundamental structure of the proposed DCPET topology is appeared in Fig. 2. It comprises of two sections: voltage-adjusting stage and confined transformation arrange. The voltage-adjusting stage is a n + 1 level voltage-adjusting converter (VBC), on the grounds that there are n arrangement capacitors and n half-extensions of the VBC. The conceivable yield voltages of the VBC are 0, Vin n , 2Vin n , . . ., and Vin. Confined change stage is an information arrangement yield parallel converter with n detached bidirectional dc–dc converters (IBDCs). In Fig. 2, there are n dc capacitors (Ci1 , Ci2 ,. . .,Cin) in arrangement start to finish, which are associated with MVdc transport Pp − Pn , and these capacitors are filled in as the info dc capacitors of the IBDCs. There are additionally n dc capacitors (Co1, Co2. . . Con) in parallel, which are associated with LVdc transport Qp − Qn , and these capacitors are filled in as the yield dc capacitors of the IBDCs. In the voltage-adjusting stage, n exchanging spans (Sp1a , Sp1b), (Sp2a , Sp2b) . . ., (Spna , Spnb) are in arrangement among Pp and Pn . (n-1) full branches (Lp1 , Cp1), (Lp1 , Cp1), . . . , (Lp(n−1), Cp(n−1)), which comprise of full inductors and capacitors are individually associated with the midpoints of the exchanging spans (Pi1 − Pin). The n + 1 level VBC can help accomplish the voltage self-adjusting in different working conditions. In the secluded change arrange, the topology of IBDC can be any past or new structure. Without loss of simplification, a full-bridge dc–dc converter is picked as the IBDC in Fig. 2.

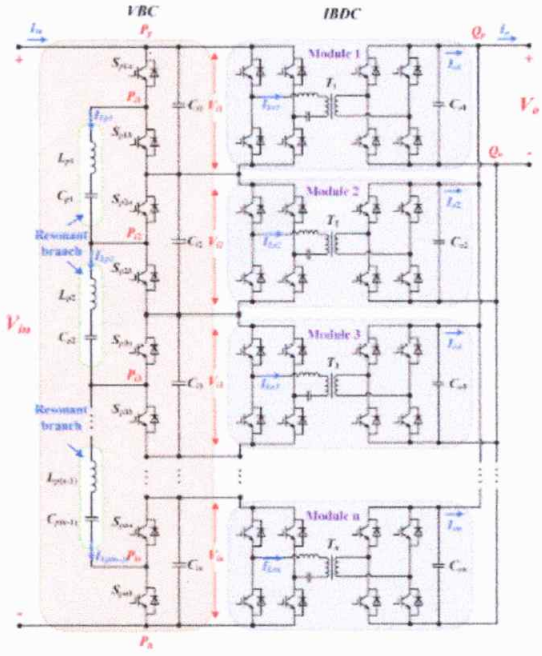


Fig. 2. Basic structure of the proposed DCPET topology.

It ought to be pointed that the topology in Fig. 2 is only a fundamental DCPET structure. In light of the fundamental topology, some other evolutional topologies can be additionally determined by alternatively changing the quantity of IBDCs as per various prerequisites, however in any event one IBDC ought to be held. At the point when some IBDCs are dispensed with, that is, the quantity of IBDCs is littler than the info dc capacitors, the voltage equalization will be guaranteed by VBC. Subsequently, the remainder of the IBDCs can at present work at an evaluated voltage. This improvement can help enormously lessen the quantity of confined transformers and switches. In the interim, when an IBDC flaw, we can legitimately locking the drive beat of the messed up IBDC to make in general PET framework proceed with regularly working and with no by-pass switch or different gadgets. At last, as a result of the voltage self-adjusting trademark, IVS control methodology can be overlooked and the control framework will be additionally rearranged. The above attributes will be talked about in detail in following segments.

B. Voltage-Balancing Converter:

For the proposed DCPET topology, VBC is utilized to guarantee voltage parity of the information arrangement dc capacitors, and is additionally filled in as a deficiency taking care of gadget. These days, the non disconnected voltage-adjusting methods are typically utilized for battery charging, which are contemplated in [30] and [31]. In this paper, a full VBC is proposed in Fig. 2. For this converter, n exchanging spans: (Sp1a , Sp1b), (Sp2a , Sp2b), . . ., (Spna , Spnb) are in arrangement with the MVdc input voltage. The resounding branches which are made out of thunderous inductors and capacitors: (Lp1 , Cp1), (Lp1 , Cp1), . . . , (Lp(n−1), Cp(n−1)) are progressively associated with the nearby midpoints (Pi1 − Pin) of the exchanging spans. The drive beats of VBC are fixed and open circle control is connected. In an exchanging period, the state of the drive heartbeats are recorded in Table I, where 1 speaks to turning ON the switches and 0 speaks to killing the switches. For investigation, a three level VBC is concentrated to represent the working standard. The topology chart is appeared in Fig. 3. Resistive burdens R1 and R2 are, separately, associated with dc capacitors Ci1 and Ci2 , which can be appeared as the dc–dc modules. At the point when R1 = R2, the voltages of Ci1 and Ci2 are equivalent. At the point when R1 = R2 , the voltages of Ci1 and Ci2 will be

extraordinary. By utilizing the VBC, the voltage equalization can be accomplished once more.

With respect to the three level VBC, assume thatR1 > R2 , the proportionate topology chart can be appeared in Fig. 3(b). From Fig. 3(b), it is shown that R1 is a typical resistive burden for each info capacitor and R1 R2 R1 −R2 is an uneven burden for Ci2 , which will add to the voltage-unequal issue. At the point when VBC is connected, the hypothetical waveforms are appeared in Fig. 4, in which, the waveforms of drive beat and thunderous current are given. On the off chance that the dead time is ignored, two working modes can be isolated in an exchanging period, which are dissected in following. Mode I (t0 − t1): At t0 , Sp1a , and Sp2a are turned ON; Sp1b and Sp2b are killed. Full capacitor Cp1 is charged by dc capacitor Ci1 through the circle, which is comprised of Sp1a , Lp1 , Cp1 and the counter parallel diode of Sp2a . In the event that the hour of this mode is a portion of the exchanging time frame 0.5Ts and the thunderous period Tr of Lp1 and Cp1 is equivalent to Ts . At that point the thunderous current will increment from 0 at t0 and diminishing to 0 again at t1,

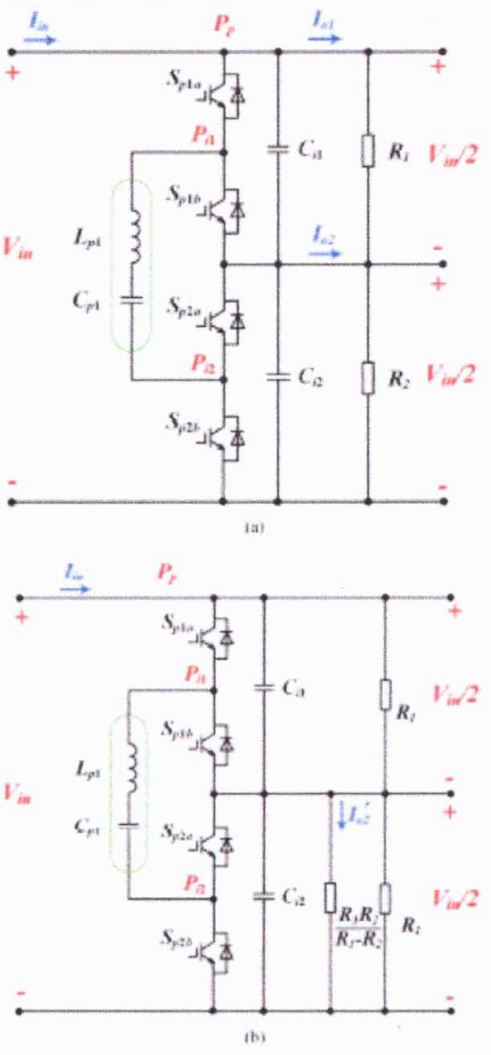


Fig. 3. Topology diagram of a three level VBC. (a) Basic topology diagram of a three level VBC. (b) Equivalent topology diagram when $R_1 > R_2$.

III.CONTROL STRATEGY:

A. Voltage and Power Control:

Concerning the regular PET with ISOP topology, the fundamental voltage and power control chart is appeared in Fig. 8. There are three control modes to control the info/yield voltage and power: voltage control mode, control mode, and hang control mode. From Fig. 8, when PET works at control mode I (voltage control mode), the information or yield voltage Vin/Vo is

estimated and contrasted and the reference esteem Vinref/Voref, at that point the distinction worth is changed over to an essential control variable dϕ by a PI controller Dv (s) to keep up the information or yield voltage consistent. At the point when PET works at control mode II (control mode), the forward or in reverse power pf/pb is estimated and contrasted and the reference esteem pfref/pbref, at that point the distinction worth is changed over to a fundamental control variable dϕ by a PI controller Dp (s) to keep up the forward or in reverse steady. At the point when PET works at control mode III (hang control mode), the control goal isn't just to keep dc transports voltage steady yet in addition to accomplish power equalization everything being equal. In this mode, the info and yield voltage reference worth can be individually communicated as

$$\begin{cases} v_{\text{inref}} = v_{\text{in}}^{*} - k_{\text{droopi}} \cdot I_{\text{in}} \\ v_{\text{oref}} = v_{o}^{*} - k_{\text{droopo}} \cdot I_{o} \end{cases} \tag{18}$$

Where v∗ in and v∗ o are the appraised estimation of information and yield voltage. With various control targets, the three control modes can be picked openly. Notwithstanding which control mode is utilized, to guarantee the power equalization of the dc–dc modules in a PET, a power-adjusting control procedure is essential. As indicated by Zhao et al. [28] and Liu et al. [37], for ISOP converter, control equalization ought to be ensured by utilizing IVS control technique. The correct side of Fig. 8 is the control graph of IVS control technique. The info voltages vi1, vi2, . . . , vin of all the dc–dc modules are, individually, contrasted and reference esteem Viaref and the balanced control factors ,Δdv1, . . . ,Δdvn are at long last determined through a PI controller Dvb(s). Where Viaref can be communicated as

$$V_{\text{iaref}} = \frac{V_{i1} + V_{i1} + \cdots + V_{\text{in}}}{n}. \tag{19}$$

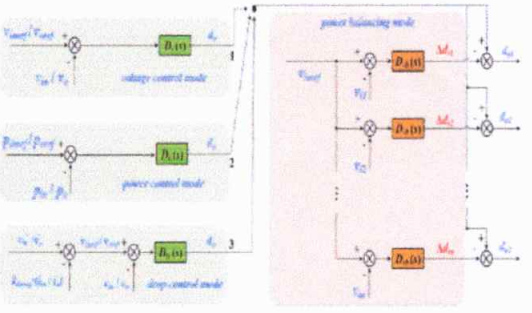


Fig. 8. Basic voltage and power control diagram for the conventional PET with ISOP topology.

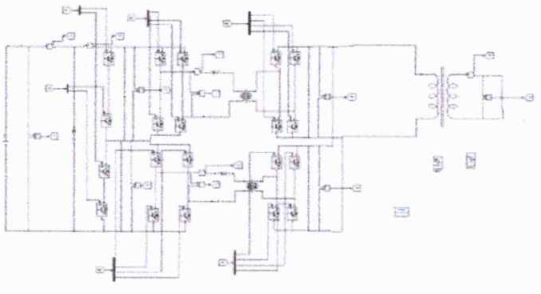
$$\begin{bmatrix} \dot{v}_{i1} \\ \dot{v}_{i2} \\ \vdots \\ \dot{v}_{\text{in}} \end{bmatrix} = \begin{bmatrix} \frac{A(s)(n-1)}{n} & -\frac{A(s)}{n} & \cdots & -\frac{A(s)}{n} \\ -\frac{A(s)}{n} & \frac{A(s)(n-1)}{n} & \cdots & -\frac{A(s)}{n} \\ \vdots & \vdots & \ddots & \vdots \\ -\frac{A(s)}{n} & -\frac{A(s)}{n} & \cdots & \frac{A(s)(n-1)}{n} \end{bmatrix} \begin{bmatrix} \dot{d}_{\varphi 1} \\ \dot{d}_{\varphi 2} \\ \vdots \\ \dot{d}_{\varphi n} \end{bmatrix} \tag{21}$$

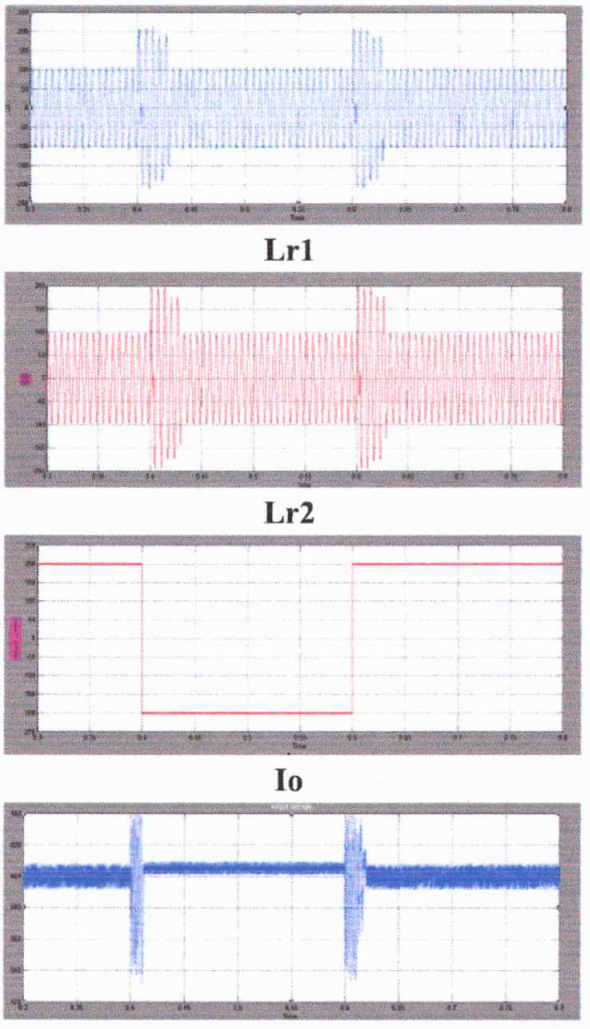
Where. It is a coupled framework for IVS control system, which is to some degree hard to plan an appropriate controller. Moreover, the unwavering quality of the control framework will be affected by utilizing IVS control system. Also, the last yield control variable dϕj is generally extraordinary as a result of conflicting

parameters of every dc–dc module, which may lead lopsided current worry of IBDCs. For the proposed novel PET topology, on the grounds that VBC is connected, input voltage self-equalization can be ensured. Hence, IVS control methodology can be dropped and just the three control modes are held, which will improve the dependability of control framework and streamline the structure technique. To dissect the control attributes, a recreation stage is constructed. The essential circuit parameters are recorded in Table II yet the info appraised voltage is 3000 V, the out evaluated voltage is 600 V, and the appraised power is 150 kW, which is utilized to mimic the down to earth application. The topologies are three-level VBC + 2 LLC RCs (n = k = 2) and three-level VBC + 1 LLC RC (n = 2, k = 1). Fig. 9 demonstrates the dynamic waveforms of the two topologies when the power stream changes from forward evaluated control +150kWto in reverse appraised power−150kW, in which the LVdc voltage is controlled. In Fig. 9, vo and io are separately yield voltage and current, ILr1 and ILr2 are the full flows of the LLC resounding converters, ILp1 is the resonant current.

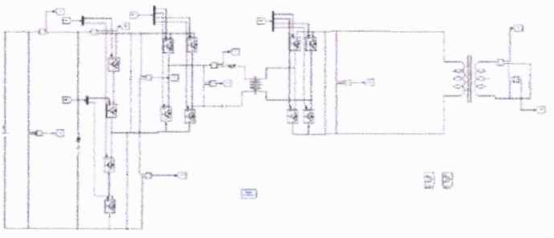
IV.SIMULATION RESULTS:

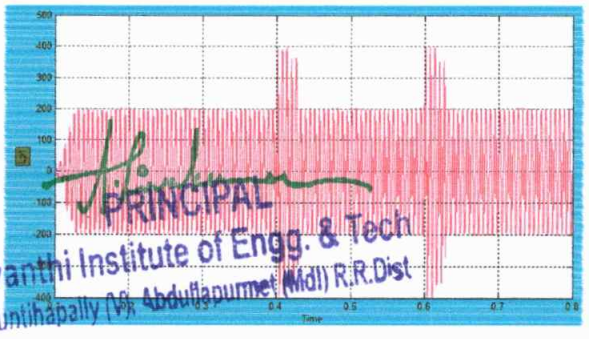
4(a) 3-level VBC + 2 LLC RCs (n=k=2).



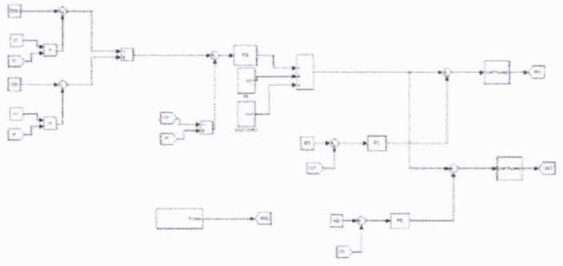


(b) 3-level VBC + 2 LLC RCs (n=k=2).

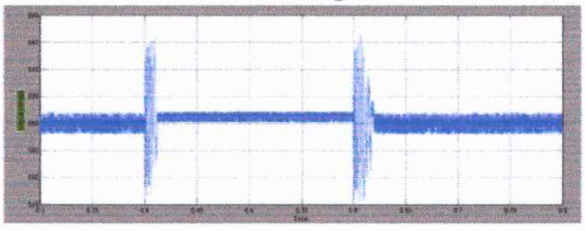




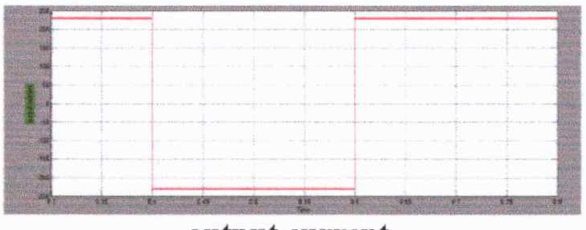
Lp1



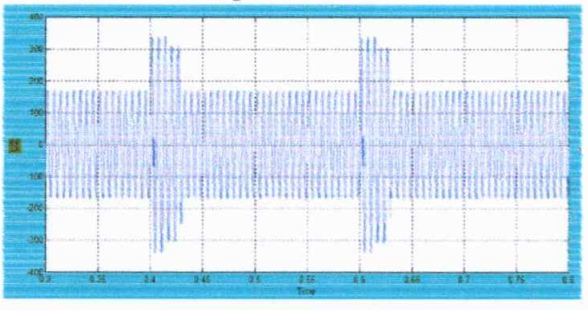
Control diagram



Lr2

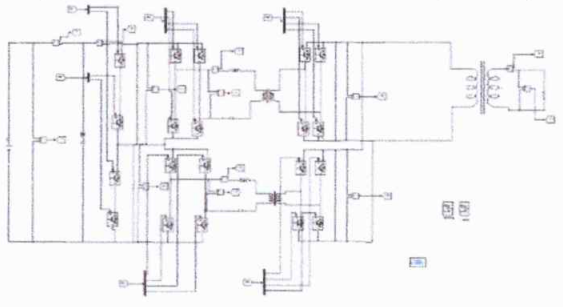


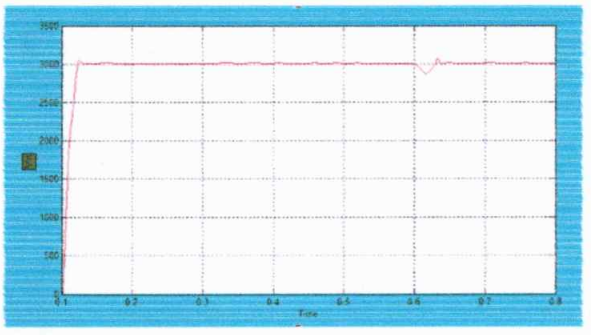
output current



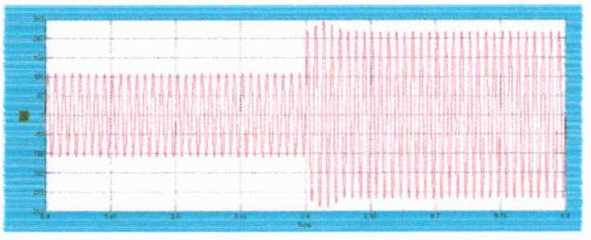
Output volyage

5(a) 3-level VBC + 2 LLC RCs (n=k=2).

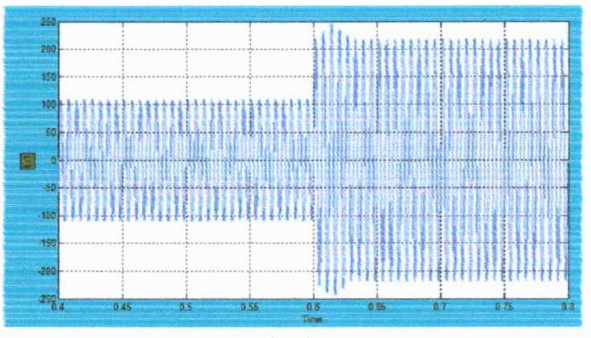




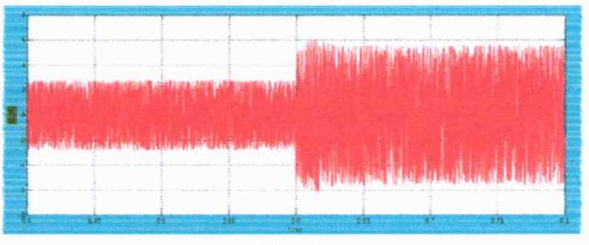
Vin



Lr2

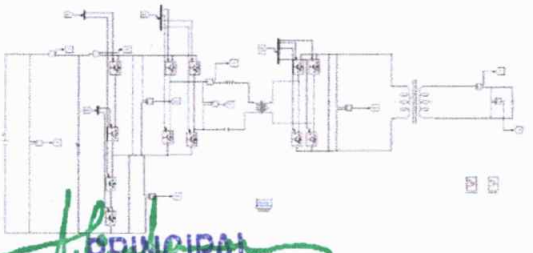


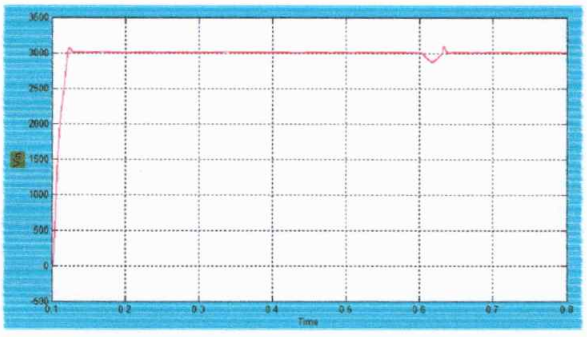
Lr1

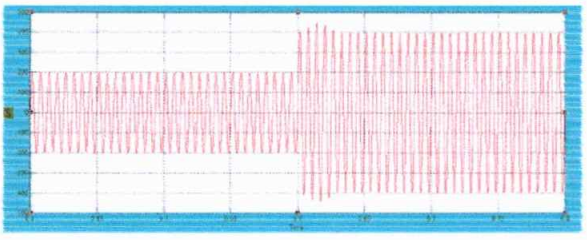


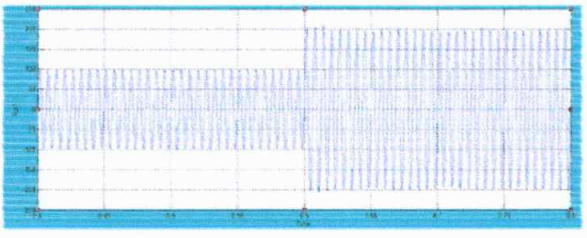
I(Lp1)

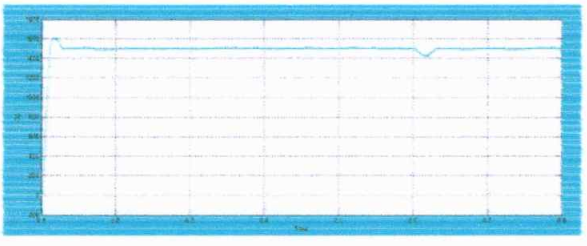
5. B level VBC + 1 LLC RC(n=2, k=1).

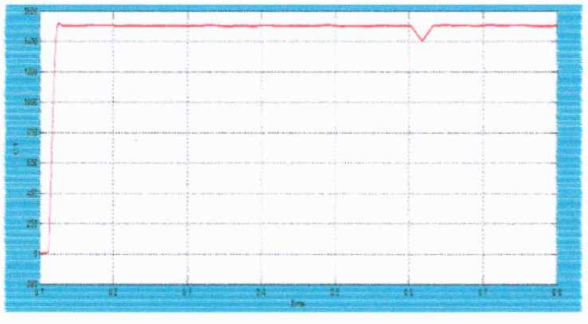












CONCLUSION: In this proposed paper we propose a novel methodology of DCPET technique to upgrade the framework arrangements. Which can't just accomplish control change between MVdc transport and LVdc transport, yet additionally be utilized in ACPET topology as a high-recurrence transformation arrange. The qualities of this topology are as per the following:

1) The quantity of the switches and transformers is productively decreased that can further diminish costs, improve control thickness, and unwavering quality.

2) The DCPET can keep working when some dc–dc modules separate and needn't bother with other shortcoming sidestep gadgets, which can improve the capacity of issue taking care of.

3) IVS control can be fail to disentangle the control framework and improve the control security.

4) The DCPET can accomplish delicate exchanging for every one of the switches, which will help increment exchanging recurrence and improve control thickness.

In view of these referenced attributes, the proposed DCPET topology can't just be utilized as a power electronic footing transformer for train to improve control thickness, yet additionally be connected for ac/dc hybrid grid or dc distribution grid to improve sinusoidal signal quality and dependability. Obviously, with the exception of these models, the proposed DCPET topology will understand other high voltage, high control applications.

REFERENCES:

[1] M. Sabahi, S. H. Hosseini, M. B. Sharifian, A. Yazdanpanah, and G. H. Gharehpetian, "A three-phase dimmable lighting system using a bidirectional power electronic transformer," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 830–837, Mar. 2009.

Page No:1706

[2] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in Proc. IEEE PES General Meet., Minneapolis, MN, USA, 2010, pp. 1–8.

[3] H. Fan and H. Li, "High frequency high efficiency bidirectional dc-dc converter module design for 10 kVA solid state transformer," in Proc. 25th Ann. IEEE Appl. Power Electron. Conf. Exp., Palm Springs, CA, USA, 2010, pp. 210–215.

[4] H. Iman-Eini, S. Farhangi, J. L. Schanen, and J. Aime, "Design of power electronic transformer based on cascaded H-bridge multilevel converter," in Proc. IEEE Int. Symp. Ind. Electron., Vigo, Spain, 2007, pp. 877–882.

[5] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," IEEE J. Emerg. Sel. Topics Power Electron., vol. 1, no. 3, pp. 186–198, Sep. 2013.

[6] Z. Li, P.Wang, Z. Chu, H. Zhu, Z. Sun, andY. Li, "A three-phase 10 kVAC- 750 VDC power electronic transformer for smart distribution grid," in Proc. 15th Eur. Conf. Power Electron. Appl., Lille, France, 2013, pp. 1–9.

[7] B. Zhao, Q. Song, J. Li, and W. Liu, "A modular multilevel DC-link front-to-front DC solid-state transformer based on high-frequency dual active phase shift for HVDC grid integration," IEEE Trans. Ind. Electron., vol. 64, no. 11, pp. 8919–8927, Nov. 2017.

[8] X. Yu, X. She, X. Zhou, and A. Q. Huang, "Power management for DC microgrid enabled by solid-state transformer," IEEE Trans. Smart Grid, vol. 5, no. 2, pp. 954–965, Mar. 2014.

[9] R. Baranwal, G. F. Castelino, K. Iyer, K. Basu, and N. Mohan, "A Dualactive-bridge-based single-phase AC to DC power electronic transformer with advanced features," IEEE Trans. Power Electron., vol. 33, no. 1, pp. 313–331, Jan. 2018.

[10] G. Buticchi, M. Andresen, M. Wutti, and M. Liserre, "Lifetime-based power routing of a quadruple active bridge DC/DC converter," IEEE Trans. Power Electron., vol. 32, no. 11, pp. 8892–8903, Nov. 2017.

[11] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "A versatile DC/DC converter based on modular multilevel converter for energy collection and distribution," in Proc. IET Conf. Renewable Power Gener, Edinburgh, Scotland, 2011, pp. 1–6.

[12] C. Zhao et al., "Power electronic traction transformer—medium voltage prototype," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3257–3268, Jul. 2014.

[13] D. Dujic et al., "Power Electronic Traction Transformer-Low Voltage Prototype," IEEE Trans. Power Electron., vol. 28, no. 12, pp. 5522–5534, Dec. 2013.

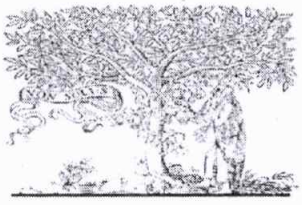
[14] J. Feng, W. Q. Chu, Z. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: challenges and opportunities," IEEE J. Emerg. Sel. Topics Power Electron., vol. 5, no. 3, pp. 1237–1253, Sep. 2017.

[15] H. Chen and D. Divan, "Soft-Switching Solid-State Transformer (S4T)," IEEE Trans. Power Electron., vol. 33, no. 4, pp. 2933–2947, Apr. 2018.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT



ELSEVIER
SSRN

IJIEMR Transactions, online available on 19th Jan 2020. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-09&issue=ISSUE-01

Title: CONTROL OF DFIG WIND POWER GENERATORS IN UNSTABLE MICROGRIDS FOUNDED ON INSTANT POWER THEORY
Volume 09, Issue 01, Pages: 46-57.

Paper Authors

AMPALLA SARITHA, MR. S.SRIKANTH REDDY

Avanthi Institute of Engineering and Technology, Hyderabad, TS, India

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl), R.R. Dist.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

CONTROL OF DFIG WIND POWER GENERATORS IN UNSTABLE MICROGRIDS FOUNDED ON INSTANT POWER THEORY

AMPALLA SARITHA[1], MR. S.SRIKANTH REDDY[2]

PG Scholar, Department of EEE (Electrical Power Systems), Avanthi Institute of Engineering and Technology, Hyderabad, TS, India.

[2]Assistant Professor, Department of EEE, Avanthi Institute of Engineering and Technology, Hyderabad, TS, India

Saritha.ampalla@gmail.com

ABSTRACT

The principle point of this paper is control methodology for a doubly-nourished enlistment generator (DFIG) wind vitality framework in an uneven microgrid dependent on momentary power hypothesis with type-2 fuzzy controller. In this task DFIG had been broadly used as a wind turbine generator, due its different preferences particularly low generation cost so it turns into the most essential and promising sources of sustainable power source. This paper introduces new control approach for a doubly-encouraged acceptance generator (DFIG) wind vitality framework in an uneven smaller scale matrix dependent on type-2 fuzzy controller. The proposed type-2 fuzzy controller utilizes immediate active/reactive power components as the framework state factors. This work focuses on studying of utilizing DFIG as a wind turbine associated with a small scale framework exposed to unbalanced loads. Moreover the control of active/reactive, the controllers utilizes the rotor-side converter for moderating the torque and reactive power pulsations. The control scheme also utilizes the framework side converter for partial compensation of unbalanced stator voltage. The primary features of the proposed control technique are its input factors are independent of reference frame transformations and it does not require sequential decomposition of current components. These features simplify the structure of required controllers under an unequal voltage condition and inherently enhance the robustness of the controllers. The execution of the proposed procedure in mitigating torque ripples and unbalanced stator voltage is examined dependent on the time-area simulation of a DFIG study framework under unequal grid voltage. Extension simulation considers are conducted to compare the response of the given framework with the type-2 fuzzy controller to the response given with the proposed plan.

Key terms: **Doubly-Fed Induction Generator, Instantaneous Power, Micro Grids, Unbalanced Grid Voltage, Wind Energy, type-2 fuzzy controller.**

I.INTRODUCTION

Wind control generation industry has ended up being commonly used over the latest couple of years and takes more thought of manufactures. There are various

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

clarifications behind adding more breeze imperativeness to the electric frameworks. For instance, wind age is maintained by not only being unblemished and manageable yet what's more having inconsequential running cost necessities. Variable speed wind turbine topologies consolidate a wide scope of generator/converter courses of action, in perspective of cost, capability, yearly imperativeness getting, and control complexity of the general system. In view of the fast redesign and progression in make of force electronic converter advancement and the enhancement of acknowledgment machines uncommonly Twofold Nourished Enlistment Generators and its inclinations of little limit of converters, high essentialness and versatile power control, DFIG has been comprehensively used for broad scale wind control age systems on account of its distinctive focal points, for instance, factor speed movement, controllable power factor and upgraded structure capability. The proportion of essentialness expelled from the breeze relies upon the event turn speed, and on the control structure associated on the breeze imperativeness change system. The DFIG is equipped with a successive power electronic converter, which can adjust the generator speed with the combination of wind speed. The converter is related with the rotor windings, which goes about as cooling excitation system. Wind turbines began to contribute and increase tenaciously in electric power age in electric frameworks. Doubly-continued acknowledgment generators (DFIGs) in high-control wind turbine-generators (WTGs) are operational as passed on generators (DGs) units in littler scale systems. Continuous structure codes require a WTG remains operational in the midst of transient and steady state uneven system voltages [1], [2].

A voltage unbalance can tenaciously exist in a scaled down scale grid in light of unequal impedance of scattering lines; nonlinear burdens, for instance, twist warmers; and unequal apportionments of single-arrange loads. Shahnia et al. in [3] propose a passed on shrewd private load trade plan to dynamically diminish voltage unbalance along low voltage allotment feeders. In any case, as a result of using comprehensively passed on and variable burdens, for instance, single-arrange motors, and nonlinear loads in a little scale network, the voltage unbalance condition can't be completely directed. Of course, even a little proportion of voltage unbalance can cause amazing current unbalance in a DFIG. This present unbalance causes torque throbs and overheating of the machine windings which over the long haul reduce the lifetime of a DFIG-based WTG in a little scale cross section [4]– [6]. Showing and vector control of DFIG-based breeze turbine under uneven conditions in little scale structures are comprehensively tended to in composing [7]– [11]. The current uneven vector control anticipates DGs routinely use two arrangements of individual controllers for the positive and negative progression portions of unbalanced streams [12]– [15]. Tuning of these controllers because of the deferrals of the separating positive/negative progressions channels every now and again

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

requires complex figurings in unequal vector control designs [14], [15].Alternative methods have been exhibited which clearly process the uneven rotor current without breaking down into positive/negative sequences[7], [8] and [16], [17]. Regardless, in these systems, the estimation of current references subject to the power throbs moreover requires the positive and negative gathering parts of the machine stator voltage, current, and change. Facilitate control (DPC) systems have been furthermore proposed for unequal voltage condition which tolerably lessen the multifaceted idea of the control technique diverged from the vector control contrive [11], [18]– 20]. Regardless, the DPC systems like the unequal vector control procedures still need breaking down of positive/negative game plans and compensation for the channels delays. This paper demonstrates a control procedure for a DFIG related with a disproportionate system voltage, which uses theprovokeactive/reactive powers as the state factors. The proposed control approach offers a solid structure since its state factors are free of the positive/negative groupings of the DFIG current parts. The prescribed control plan also reduces the DFIG torque/control throbs by using the active/reactive power bearings of the rotor-side converters in a DFIG wind essentialness system. Besides, at low breeze speed and high unequal system voltage conditions, the plenitude furthest reaches of grid side converter can be used for fragmentary pay of uneven stator voltage. Two current/control limiting computations are similarly exhibited for both rotor-and system side converters to avoid over rating of the converters. The execution of the proposed system under disproportionate network voltage condition is inquired about by methods for time-space reenactment of a MW-scale DFIG wind turbine-generator examine structure in which a single stage stack is used to compel a persistent voltage unbalance to the small scale framework.

II. CONVENTIONAL VECTOR CONTROL SCHEME FOR DFIG SYSTEM

Fig1 exhibits the schematic layout of a DFIG WTG including rotor-side (RSC) and network side (GSC) converters. Under organized subject to common vector control or other arrangement techniques, for instance, resonation controller and direct power control using fleeting force model of the DFIG [17], [21]. In any case, under unequal voltage condition, right hand control circles using negative game plans sums must be added to the standard vector speed controllers which outline a comprehensive disproportionate vector control contrive [7], [17].Figure 2 demonstrates nuances of the uneven vector control plot for the rotor-side converter [12], [13]. This control procedure mitigates the torque throbs and the framework unequal effects on the generator by methods for independent control of the stator real/responsive power parts, p∗s and q∗s. The progressive crumbling unit in Fig. 2 registers the positive/negative game plan

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

parts in positive/negative progression qd reference outline.

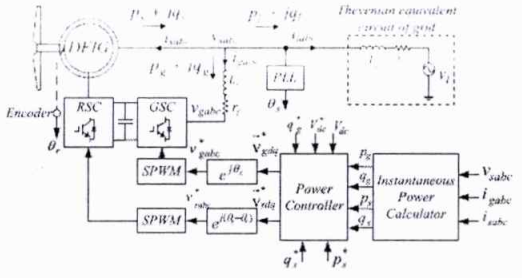


Fig 1. Schematic diagram of DFIG-based Wind Generation System.

Fig. 2, the uneven vector control technique is built up dependent on decompensation of the positive and negative successions of the rotor current. For all intents and purposes, this decay can be acknowledged by exchanging the current to the synchronous reference edge and utilizing computerized channels, or flag defer cancelation strategy. These strategies present time delays and evident blunders in adequacy and stage which antagonistically influence on the dynamic execution of the control framework [20].

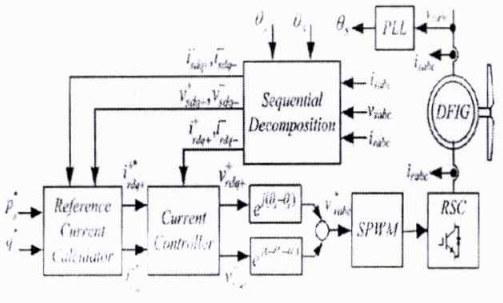


Fig 2. Schematic diagram of the conventional unbalanced vector control scheme for DFIG.

III. PROPOSED CONTROLLER FOR UNBALANCED VOLTAGE CONDITIONS

A. Instantaneous Power Model of a DFIG

The model of the induction machine in terms of the stator real/reactive power components, psand qs is

$$\frac{d}{dt}\begin{bmatrix} p_s \\ q_s \\ \psi_{sd} \\ \psi_{sq} \end{bmatrix} = \begin{bmatrix} g_1 & -\omega_s & -g_4 & -g_5 \\ \omega_s & g_1 & -g_5 & g_4 \\ \frac{2r_s r_g}{3|v_s|^2} & \frac{2r_s v_g}{3|v_s|^2} & 0 & \omega_r \\ \frac{2r_s v_g}{3|v_s|^2} & -\frac{2r_s r_g}{3|v_s|^2} & -\omega_r & 0 \end{bmatrix} \begin{bmatrix} p_s \\ q_s \\ \psi_{sd} \\ \psi_{sq} \end{bmatrix} + \begin{bmatrix} u_{sd} \\ u_{sq} \\ v_{sd} \\ v_{sq} \end{bmatrix} \quad \ldots\ldots 1$$

where subtleties of urd,rq and g1 to g7 are given in Appendix. The lattice side converter and channel demonstrate as far as prompt genuine and responsive intensity of network side converter, pg and qg, is

$$\begin{bmatrix} \frac{dp_g}{dt} \\ \frac{dq_g}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_f}{l_f} & -\omega_e \\ \omega_e & -\frac{r_f}{l_f} \end{bmatrix} \begin{bmatrix} p_g \\ q_g \end{bmatrix} + \frac{1}{l_f} \begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} \quad \ldots\ldots 2$$

Where

$$u_{gd} = \frac{3}{2}\left(|V_s^2| - \left(V_{gd}V_{sd} + V_{gq}V_{sq}\right)\right) \quad \ldots\ldots..3$$

And

$$u_{gd} = \frac{3}{2}\left(V_{gq}V_{sd} - V_{gd}V_{sq}\right) \quad \ldots.4$$

The dynamic model of the dc link is:

$$\frac{dv_{dc}}{dt} = \frac{i_{dc\_}P_G - p_r}{C \quad CV_{dc}} \quad \ldots\ldots 5$$

where the real power delivered to the rotor, pr, is:

$$p_r = \frac{3}{2}\left(v_{rd}i_{rd} + v_{rq}i_{rq}\right) \quad \ldots.6$$

Equations (1)-(6) summarize the model of a DFIG wind power system including the machine and converters.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

B. Compensation of Unbalanced Voltage Utilizing GSC

The excess furthest reaches of system side converter at low breeze speed can be used for a midway compensation of uneven stator voltage. This can be practiced through the control of the authentic/open power in GSC contrasting with the negative gathering of the cross section voltage. This zone develops the logical association between the power throb and the negative course of action voltage which is required in the structure technique for the control system. The current/voltage vectors can be imparted the extent that their game plan parts in +/ - synchronous reference traces as:

$$f^{+}_{dq} = f^{+}_{dq} + f^{+}_{dq} = f^{+}_{dq} + f^{-}_{dq} - e^{-j\omega e^{t}}$$

.....7

Based on(7), the instantaneous real/reactive power components can be obtained via definition of complex power as:

$$s_g(t) = p_g(t) + jq_g(t) = \frac{3}{2} v^{+}_{sdq} i^{+}_{gdq}$$

$$\frac{3}{2}(v^{+}_{sdq} + i^{+}_{gdq} - e^{-j2\omega e^{t}})(i^{+}_{gdq} + i^{-}_{gdq} - e^{j2\omega e^{t}})$$

$$= \frac{3}{2}(v^{+}_{sdq} i^{+}_{gdq} + v^{-}_{sdq} i^{-}_{gdq-})$$

$$+ \frac{3}{2}(v^{+}_{sdq} + i^{-}_{gdq} - e^{j2\omega e^{t}} + v^{-}_{sdq} - i^{+}_{gdq} + e^{-j2\omega} e^{t}$$

...8

Fig3 demonstrates the schematic graph of the framework side converter model and DFIG regarding power segments dependent on (1) and (16)- (22). In this model, control throb references for GSC are utilized for modifying the negative grouping lattice voltage.

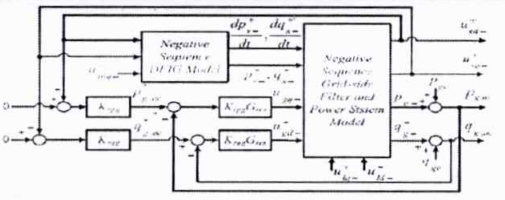


Fig3. Schematic diagram of the GSC model for compensating the negative sequence of the grid voltage

Figure 4 portrays the proposed control framework for matrix side converter. In this control framework, GPg, Gqg and Gdc controllers are structured dependent on adjusted model as explained in [21]. At that point, additional control circles including Kvdg, Kvqg, KrpgGres and KrqgGres are utilized to control throbs of converter relating to throbs of lattice voltage at positive succession reference outline. The full compensator (Gres) tuned at the twofold recurrence of the matrix which is actualized in the positive succession reference outline. The step channel Gnf is additionally utilized for stifling the dc-interface voltage twofold recurrence (2ωe) swell. The exchange elements of resounding compensator and step channel (Gnf) which are tuned at ω0 = 2ωe recurrence are:

$$G_{res} = \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad G_{res} = \frac{s^2 + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

....9

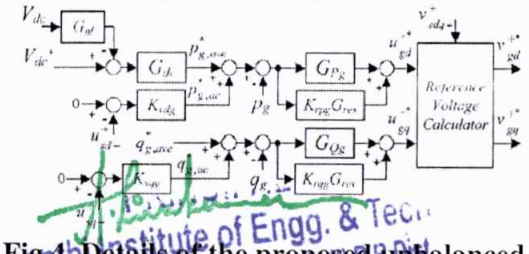


Fig 4. Details of the proposed unbalanced controllers for the grid-side converter.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

C. Mitigation of Torque/Reactive Power Pulsations Using RSC

In spite of the fact that GSC to some degree can remunerate the uneven matrix voltage, the torque and power throbs still exist because of 2ωe swell which superimposed on the dc-connect voltage. The torque throb in a generator expands weight on the pivoting shaft of the DFIG which can cause shaft weariness or other mechanical harms to a WTG. Subsequently, a control arrangement is required for the rotor-side converter to alleviate the torque/control throbs of DFIG. Santos-Martin et al. in [23] demonstrate that the concurrent end of the torque and genuine power throbs can't be performed under uneven framework voltage condition. In this way, the proposed control plot thus is intended to remunerate the torque and receptive power throbs as appeared in Fig. 5.Krps, Krqsand Kr Teare steady gains and Gresis a band pass channel tuned at twofold recurrence as given in (23). The electric torque can be evaluated by stator and rotor flow parts in the stationary reference outline as

$$T_e = \frac{3pL_m}{2}\left(i_{sQ}i_{rD} - i_{sD}ir_Q\right) \quad \ldots.10$$

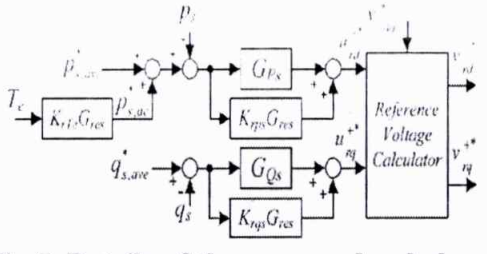


Fig 5. Details of the proposed unbalanced controllers for the rotor-side converter.

IV. DESIGN OF TYPE-2 FUZZY LOGIC CONTROLLER

At the point when a framework has impressively vast sureness, Type 1 Fuzzy Logic Controller (T1FLC) can't achieve the ideal dimension of execution with a reasonable multifaceted nature of the structure. In such cases, the utilization of Type 2 Fuzzy Logic Controller (T2FLC) is prompted as the good FLC in the examinations in territories, for example, determining of time-arrangement, controlling of portable robots, the truck backing-up control issue, Very Large Scale Integration (VLSI) and Field Programmable Logic Devices (FPGA) .Executions of T2FLC uncovers that when the parameters are suitably balanced, T2FLC can result in a superior capacity to foresee when contrasted with T1FLC [Liang Q and Mendel J. M (2000)]. For machines like continuous portable robots, T2FLCs are most appropriate application. For the instance of continuous usage, writing overview demonstrates that a customary T1FLCs can't deal with the vulnerabilities in the framework effectively and a T2FLC utilizing type-2 fuzzy sets results in a superior execution. Likewise, by utilizing T2FLC the amount of controls to be resolved additionally diminishes in spite of the fact that the parameters to be resolved don't get decreased.

Hagras, H. (2007) displayed that Type-2 fuzzy sets are finding wide appropriateness in guideline based fuzzy rationale

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

frameworks (FLSs) in light of the fact that they let vulnerabilities be demonstrated by them though such vulnerabilities can't be displayed by Type-1 fuzzy sets. A square graph of a Type-2 Fuzzy Logic System (T2FLS) is portrayed in Figure 5.1.

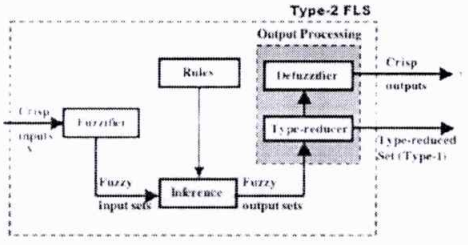


Figure 6: Block diagram of Type-2 Fuzzy Logic System

In the square chart, there is an additional square - type reducer, which is absent in Type-1 FLS yet is required in Type-2 FLS structure. In spite of the fact that the Type 2 FLS has a few points of interest when managing vulnerabilities, however it likewise expands the numerical computation.

The squares of Type 2 FLS are as:

a) Fuzzifier: The fuzzifier maps fresh contributions to Type-2 fuzzy sets which enacts the deduction motor.

b) Rule base: The principles in a T2FLS and T1FLS are same, yet predecessors and consequents are spoken to by Type-2 fuzzy sets.

c) Inference: Inference square doles out fuzzy contributions to fuzzy outputs utilizing the guidelines in the standard base and the administrators, for example, association and crossing point.

d) Type-decrease: The Type-2 fuzzy outputs of the deduction motor are changed into Type-1 fuzzy sets that are known as the sort diminished sets. There are two normal techniques for the sort decrease activity in the T2FLSs: One is the Karnik-Mendel cycle calculation, and the other is Wu-Mendel vulnerability limits strategy.

e) Defuzzification: The second step of yield handling, which happens after sort decrease, is still called defuzzification. Since a sort decreased arrangement of an Interval type-2 fuzzy set is dependably a limited Interval of numbers, the defuzzified esteem is only the normal of the two end-purposes of this Interval.

V.SIMULATION RESULTS

MATLAB/SIMULINK results are introduced in this area for approving unfaltering state and dynamic exhibitions of this proposed DFIG with incorporated dynamic channel capacities.

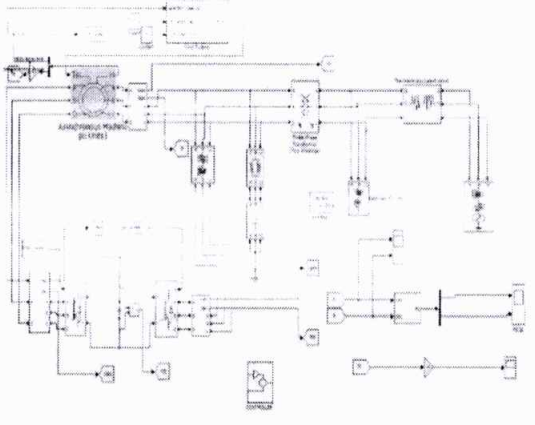


Fig 7.MATLAB.SIMULINK diagram of proposed type-2 fuzzy controller based DFIG

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

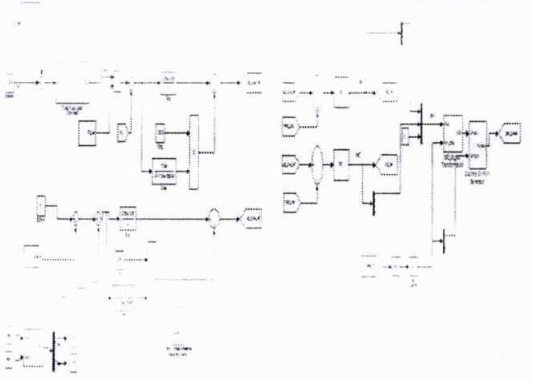


Fig 8.Grid side Controller with Type-2 Fuzzy controller

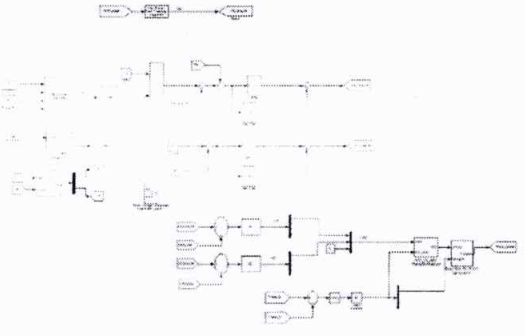
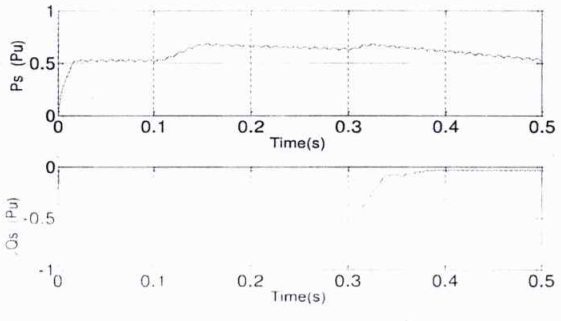
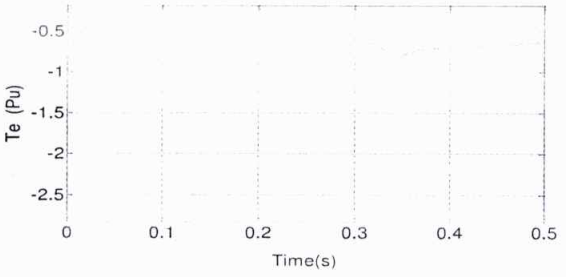


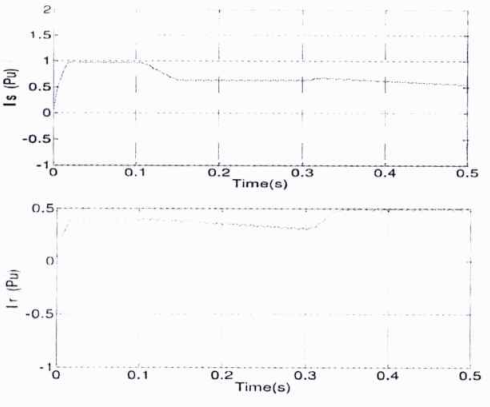
Fig 9.Rotor side Controller with Type-2 Fuzzy controller



(a) stator real power; (b) stator reactive power;

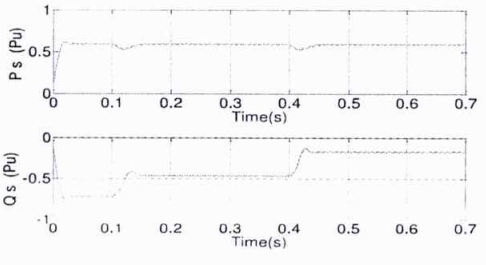


(c) Torque;



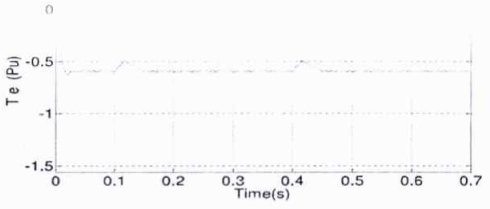
(d) stator and rotor currents.

Fig 10.The DFIG performance under unbalanced voltage using balanced controller

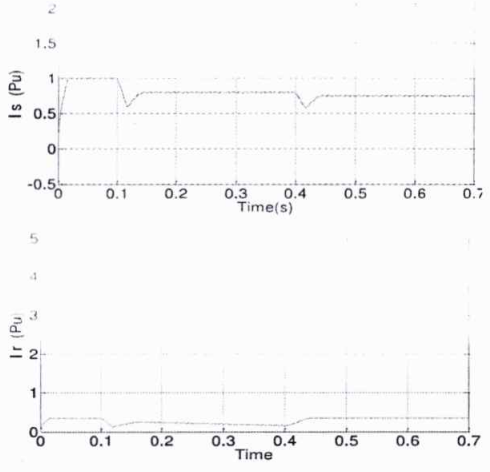


(a) stator real power; (b) stator reactive power;

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

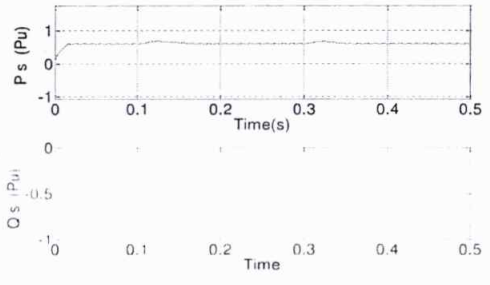


(c) torque;

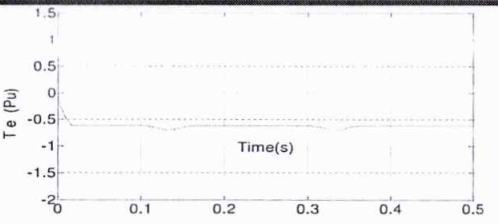


(d) Stator and rotor currents.

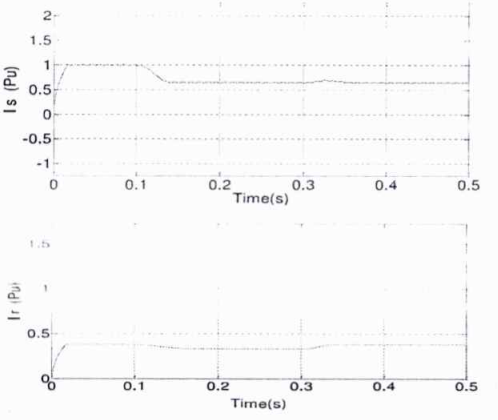
Fig. 11. Unbalanced vector controller:



(a) Stator real power; (b) stator reactive power;

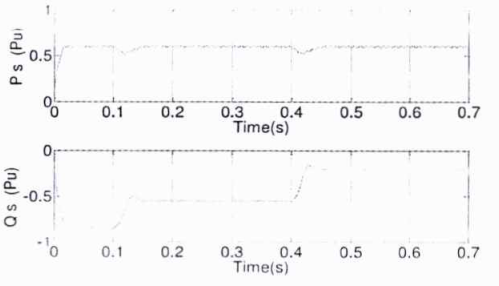


(c) Torque;



(d) Stator and rotor currents.

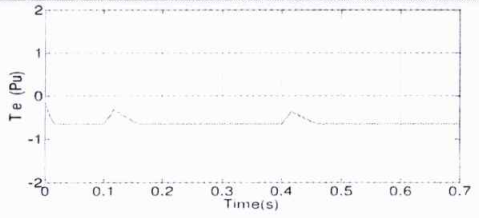
Fig.12. the proposed controller



(a) Stator real power;(b) stator reactive power;

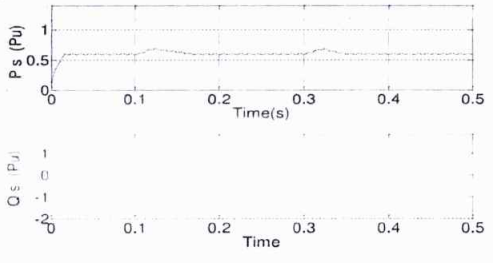
PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

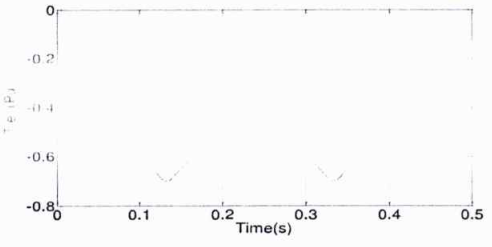


(c) Torque.

Fig.13. Robustness of the unbalanced vector controller:

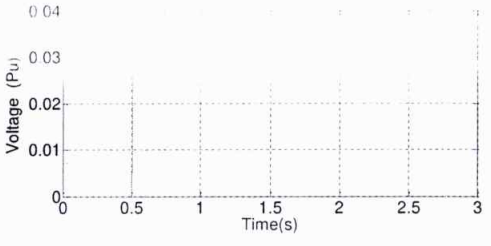


(a) Stator real power; (b) stator reactive power;

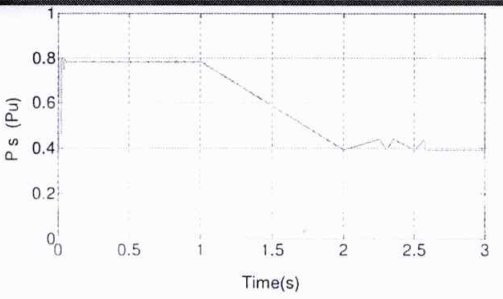


(c) Torque.

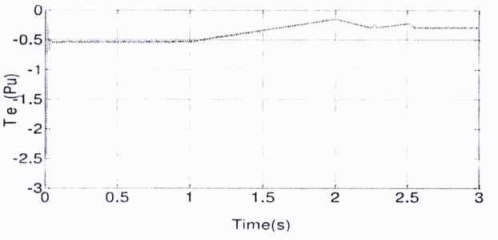
Fig.14. Robustness of the proposed controller:



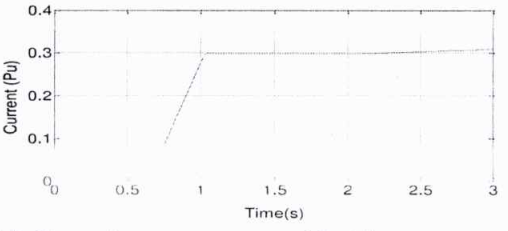
(a) Negative sequence of the stator voltage;



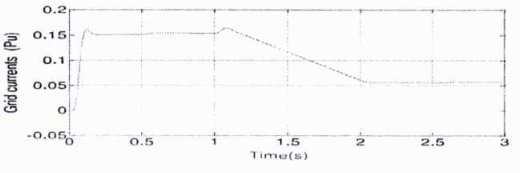
(b) Stator real power;



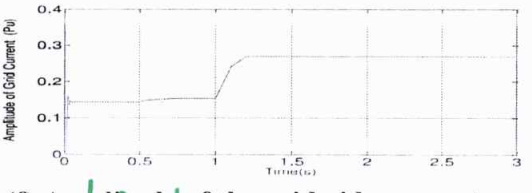
(c) Torque;



(d) Negative sequence grid-side converter current.



(e) Positive sequence grid-side converter current;



(f) Amplitude of the grid-side converter current.

Fig.15. Partial compensation of unbalanced stator voltage

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

CONCLUSION

A DFIG wind turbine-generator with Type-2 Fuzzy controller has been introduced in this paper which does not require the successive decay of the DFIG stator/rotor flows and is less sensitive to the framework parameters. This control method mitigates the stator reactive power and torque ripples which obviously appear in any balanced control scheme under an unbalanced grid voltage condition. The control strategy utilizes the grid side converter to in part remunerate the unbalance stator voltage when the wind speed is low and turbine works below nominal power. It has been demonstrated that proposed control approach dependent on its basic and robust structure can offer a promising solution for DFIG control under unbalanced grid voltage conditions. In the extension proposed Type-2 fuzzy controller.The traditional type-1 FLCs that use crisp type-1 fuzzy sets cannot directly handle such uncertainties. Type-2 FLCs that utilize type-2 fuzzy sets can handle such uncertainties to produce a better performance. Hence, type-2 FLCs will have potential to overcome the limitations of type-1 FLCs and produce a new generation of fuzzy controllers with enhanced performance for many applications which require handling high levels of uncertainty.

VIII. REFERENCES

[1] M. Mohseni and S. M. Islam, "Review of international grid codes for wind power integration: Diversity, technology and a case for global standard," Renew. Sustain. Energy Rev., vol. 16, no. 6, pp. 3876–3890, 2012

[2] C. Jauch, J. Matevosyan, T. Ackermann, and S. Bolik, "International comparison of requirements for connection of wind turbines to power systems," Wind Energy, vol. 8, no. 3, pp. 295–306, 2005.

[3] F. Shahnia, P. J. Wolfs, and A. Ghosh, "Voltage unbalance reduction in low voltage feeders by dynamic switching of residential cus-tomers among three phases," IEEE Trans. Smart Grid, vol. 5, no. 3,pp. 1318–1327, May 2014.

[4] R. Piwkoet al., "Integrating large wind farms into weak power grids with long transmission lines," in Proc. CES/IEEE 5th Int. Power Electron.Motion Control Conf. (IPEMC), vol. 2. Dalian, China, 2006, pp. 1–7.

[5] K. Lee, T. M. Jahns, W. E. Berkopec, and T. A. Lipo, "Closed-form analysis of adjustable-speed drive performance under input-voltage unbalance and sag conditions," IEEE Trans. Ind. Appl., vol. 42, no. 3,pp. 733–741, May/Jun. 2006.

[6] E. Nasr-Azadani, C. A. Cañizares, D. E. Olivares, and K. Bhattacharya, "Stability analysis of unbalanced distribution systems with synchronous machine and DFIG based distributed generators," IEEE Trans. Smart Grid, vol. 5, no. 5, pp. 2326–2338, Sep. 2014.

[7] H. Xu, J. Hu, and Y. He, "Integrated modeling and enhanced control of DFIG under unbalanced and distorted grid voltage conditions," IEEETrans. Energy Convers., vol. 27, no. 3, pp. 725–736, Sep. 2012.

[8] J. Hu and Y. He, "DFIG wind generation systems operating with limited converter rating considered under unbalanced network

conditions—Analysis and control design," Renew. Energy, vol. 36, no. 2,pp. 829–847, 2011.

[9] Y. Yan, M. Wang, Z.-F. Song, and C.-L. Xia, "Proportional-resonant control of doubly-fed induction generator wind turbines for low-voltage ride-through enhancement," Energies, vol. 5, no. 11, pp. 4758–4778, 2012.

[10] C. Liu, F. Blaabjerg, W. Chen, and D. Xu, "Stator current harmonic control with resonant controller for doubly fed induction generator," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3207–3220, Jul. 2012.

[11] P. Zhou, Y. He, and D. Sun, "Improved direct power control of a DFIG-based wind turbine during network unbalance," IEEE Trans. Power Electron., vol. 24, no. 11, pp. 2465–2474, Nov. 2009.

[12] Y. Zhou, P. Bauer, J. A. Ferreira, and J. Pierik, "Operation of grid-connected DFIG under unbalanced grid voltage condition," IEEE Trans. Energy Convers., vol. 24, no. 1, pp. 240–246, Mar. 2009.

[13] L. Xu and Y. Wang, "Dynamic modeling and control of DFIG-based wind turbines under unbalanced network conditions," IEEE Trans. Power Syst., vol. 22, no. 1, pp. 314–323, Feb. 2007.

[14] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary control scheme for voltage unbalance compensation in an islanded droop-controlled micro grid," IEEE Trans. Smart Grid, vol. 3, no. 2,pp. 797–806, Jun. 2012.

[15] M. Hamzeh, H. Karimi, and H. Mokhtari, "Harmonic and negative-sequence current control in an islanded multi-bus MV micro grid," IEEETrans. Smart Grid, vol. 5, no. 1, pp. 167–176, Jan. 2014.

[16] L. Xu, "Enhanced control and operation of DFIG-based wind farms during network unbalance," IEEE Trans. Energy Convers., vol. 23, no. 4,pp. 1073–1081, Dec. 2008.

[17] V.-T. Phan and H.-H. Lee, "Performance enhancement of stand-alone DFIG systems with control of rotor and load side converters using resonant controllers," IEEE Trans. Ind. Appl., vol. 48, no. 1, pp. 199–210, Jan./Feb. 2012.

[18] G. Abad, M. A. Rodriguez, G. Iwanski, and J. Poza, "Direct power control of doubly-fed-induction-generator-based wind turbines under unbalanced grid voltage," IEEE Trans. Power Electron., vol. 25, no. 2,pp. 442–452, Feb. 2010.

[19] J. Alonso-Martinez, J. Eloy-Garcia, D. Santos-Martin, and S. Arnaltes, "A new variable-frequency optimal direct power control algorithm," IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1442–1451, Apr. 2013.

INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY
ISSN [O]: 2582-1431 VOLUME-II ISSUE-II APR-JUNE-2020

MITIATION OF VOLTAGE SAG USING DYNAMIC VOLTAGE RESTORER (DVR)

T.Kranthi Kumar
Assoc.Professor and Head in Department of EEE,Avanthi institute of engineering & Technology(JNTUH).
Email: kranthikumarthallapalli@gmail.com
Reddy Srikanth
PG Student in Department of EEE,Avanthi institute of engineering & Technology(JNTUH).
Email:reddysrikanth.vgse@gmail.com

***Abstract*— Various factors that affect the power quality are voltage unbalance, presence of harmonics, interruptions, the occurrence of faults, and the presence of voltage sag and voltage swell. Out of all the power quality issues, the presence of voltage sags is the critical problem. To address the issues of power quality, special devices are available, which are called flexible alternating current transmission system (FACT) devices. In this paper , various power quality issues are presented. Among all, the occurrence of voltage sag is studied and analyzed. The control circuit to mitigate the voltage sag issues is modeled and simulated. The dynamic voltage restore is used to compensate for the voltages that fall out of the limits. The entire analysis is carried out in MATLAB/SIMULINK. The detailed model for the dynamic voltage restorer is also presented. The circuit topology, control logic, various subsystems, and generation of the voltage sag are important aspects of this paper.**

***Index Terms*— power quality ,voltage sag , voltage swell, dynamic voltage restore**

I. INTRODUCTION

Due to the development of semiconductor technology, the era of power electronics is changed drastically. Newer elements and devices with fast response characteristics and with compact size have emerged. Due to the attractive features of those elements/devices, the control of power became easy and flexible. Various applications of the semiconductor elements are shown in the figure below. Most of the commercial, industrial, and domestic loads are designed with these kinds of elements. The entire system is occupied by the semiconductor elements. Despite the advantages of modern semiconductor elements, the major drawback is, they impose nonlinearity into the system. Due to the non-linear property of those elements, a lot of issues are present in electrical power. The issues are not only limited to the electrical distribution system but also extended to the power transmission system. Those issues affect the quality of electrical power. So, they are called power quality issues/problems.

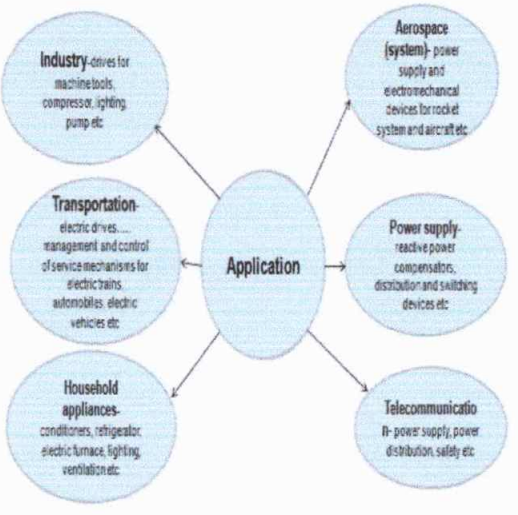


Figure 1 Applications of modern semiconductor devices

The reactive power compensation technique is used in FACTs devices. There are two components of electrical power. The active power and reactive power. The active power is consumed by all loads, whereas loads do not consume reactive power. The disturbances in real or active power can be suppressed using the unused reactive power. This technique is known as reactive power compensation. All the FACTs devices work on the same technique, even though different devices will provide a solution to different problems.

A. *Types in FACTs Devices*

The FACTs devices are classified based on the connection in the lines. By considering that factor, they are classified as the following types

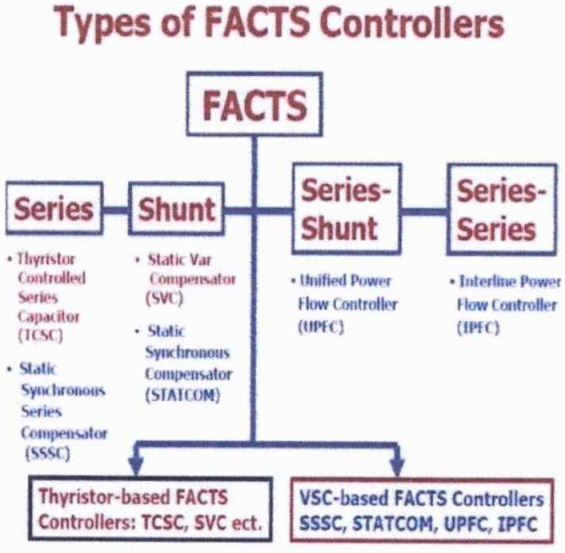


Figure 2 FACTS classification

B. *Compensation by FACTs*

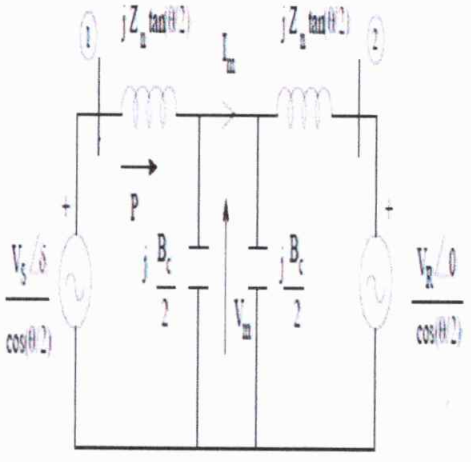


Figure 3 Equivalent circuit of shunt compensation

The above circuit shows the equivalent circuit of the shunt compensation in lines. Two capacitors connected across the line are used as the reactive power sources in shunt compensation. Half of the capacitance is near the first end, and the remaining half is placed near the second end. Usually, the first end is the source end or sending end. The second end is load end or receiving end.

II. VOLTAGE SAG ANALYSIS

A. *Duration and Magnitude*

The magnitude and duration are the most important characteristics of voltage sag. These parameters are defined as follows

- The amplitude of the voltage drop in the system is called the sag magnitude
- The time for which the magnitude is lower than the actual system voltage is called the duration of the sag

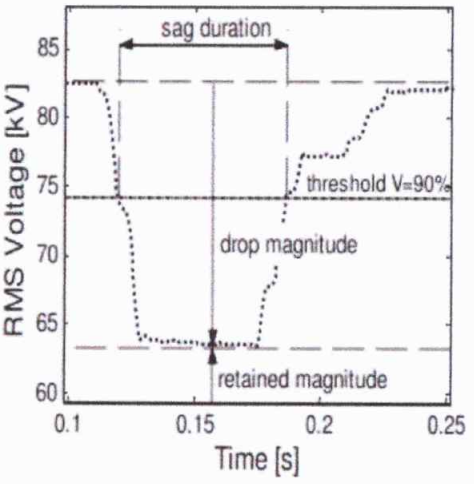


Figure 4 sag properties

Table 1 Classification of sag according to IEEE 1159

Type of Sag	Duration	Magnitude
Instantaneous	0.5 - 30 cycles	0.1 - 0.9 pu
Momentary	30 cycles - 3 s	0.1 - 0.9 pu
Temporary	3 s - 1 min	0.1 - 0.9 pu

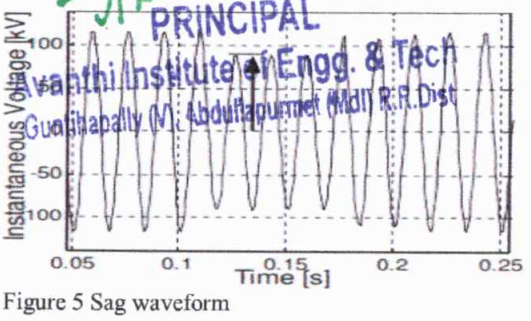


Figure 5 Sag waveform

III. DYNAMIC VOLTAGE RESTORER (DVR)

The dynamic voltage restoration process is presented using the dynamic voltage restorer device. The configuration of the DVR is shown in the figure below.

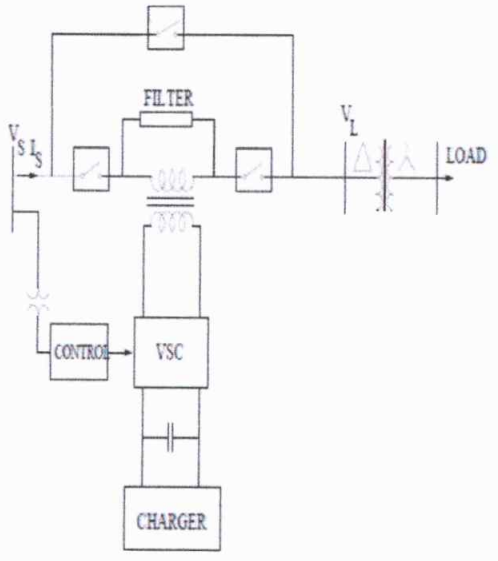


Figure 6 Structure of DVR

A. Operation

The DVR can be operated as a series compensating device. It can be operated in combination with a voltage source converter to get the best results in improving the power quality issues. DVR has the following operating modes

- Standby mode
- Boosting mode

During the first mode of operation, it will not inject any voltage into the system. Only it will be in standby mode. Whereas, in the second mode, the DVR injects the voltage into the system for voltage compensation.

The DVR requires the continuous operation of following the following subsystems

- Boost transformers
- Passive filtering equipment
- Energy storage device
- Control circuit

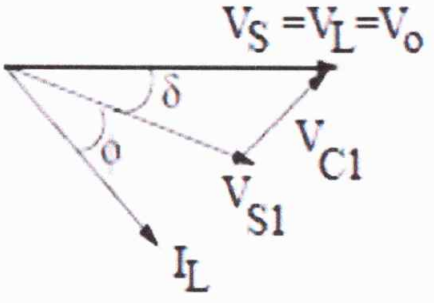


Figure 7 DVR injected voltage

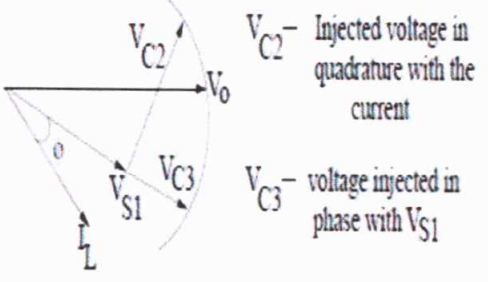


Figure8 Alternate control logic

B. Protection and control

While mitigating the voltage sags and the other voltage compensation, it has to consider the following things.

- The energy storage system is ON during standby mode so that DVR will operate in self-charging mode.
- During sag/swells, it has to inject the voltage into the system. In that injected voltage, the presence of zero sequences is not required.
- It should have appropriate protection equipment to protect from sudden short

circuits. So the breakers and other protection equipment need to be used.

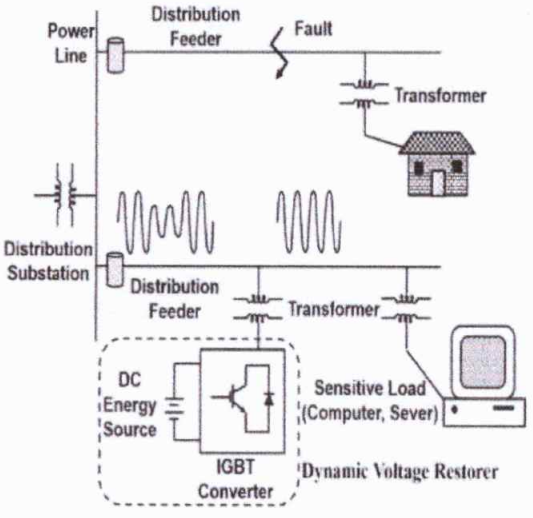


Figure 9 Installation of DVR

IV. SIMULATION RESULTS

the simulation results obtained for the dynamic voltage restorer for suppression of voltage sag is presented. Entire simulations are carried out in MATLAB/SIMULINK. The results are shown for the single-phase and three-phase systems.

A. Sytem Specification

The following are the system specification. The system considered here is the single- phase system; it consists of the following specification.

- A fault occurs at 0.015s to 0.27s, during this the voltage sag occurs
- A fault occurs at 0.37s to 0.43s, during this the voltage swell occurs
- The supply voltage is 230 V RMS.
- The inductive load is used in the simulation
- The step size used in the simulation is 1e-5.

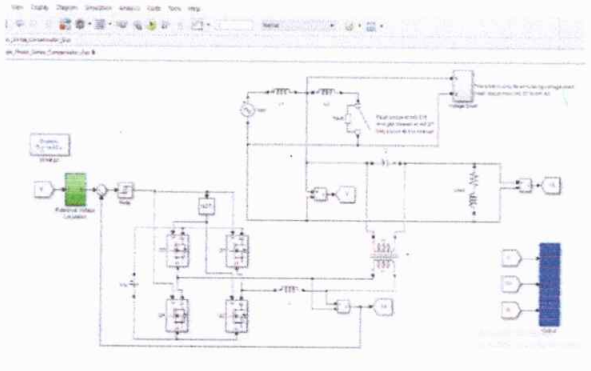


Figure 10 Single-phase DVR for mitigation of Voltage sags and Swells

B. Output waveforms of Single phase

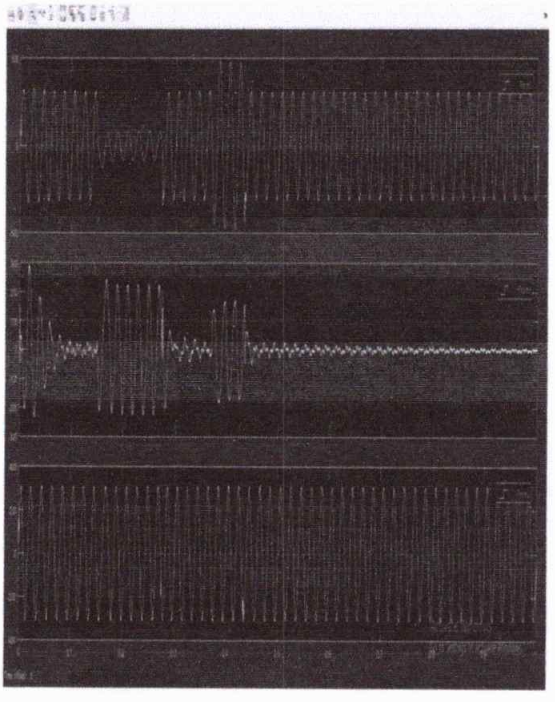


Figure 11 Supply voltage, reference voltage, and the output voltage of DVR

In the above figure, the first waveform shows supply voltage, in which voltage sag and swell are present.

- The second figure shows the reference voltage generated by DVR, which is injected into the system; only during voltage sag and swell, the magnitude of the reference voltage is maximum; otherwise, it is minimum.
- The third waveform shows the output voltage at the load terminals, irrespective of the presence of voltage sags and swells; the output is like a pure sinusoidal waveform.
- From the sinusoidal voltage, it can be stated that the presence of dynamic voltage restorer suppresses the voltage sags and swells.

V. CONCLUSION

Following are the conclusions of the present work carried out in this report

- DVR is the best device to mitigate the voltage sags and swells in the lines
- The sags that occur in transformer are not possible to suppress
- The sag and swell generation mechanism is different
- The DVR response for voltage sags and swells in equal.

REFERENCES

1. Bajaj, Mohit. "Design and Simulation of Hybrid DG System Fed Single-Phase Dynamic Voltage Restorer for Smart Grid Application." *Smart Science* 8, no. 1 (2020): 24-38.
2. Ansal, Valappil. "ALO-optimized artificial neural network-controlled dynamic voltage restorer for compensation of voltage issues in distribution system." *Soft Computing* 24, no. 2 (2020): 1171-1184.
3. Pal, Rakeshwri, and Sushma Gupta. "Topologies and Control Strategies Implicated in Dynamic Voltage Restorer (DVR) for Power Quality Improvement." *Iranian Journal of Science and Technology, Transactions of Electrical Engineering* 44, no. 2 (2020): 581-603.
4. Molla, Emiyamrew Minaye, and Cheng-Chien Kuo. "Voltage Sag Enhancement of Grid Connected Hybrid PV-Wind Power System Using Battery and SMES Based Dynamic Voltage Restorer." *IEEE Access* 8 (2020): 130003-130013.
5. Rosli Omar, N.A. Rahim and Marian Sulaiman, "Dynamic Voltage Restorer Application for Power Quality Improvement in Electrical Distribution System: An Overview," Australian Journal of Basic and Applied Sciences, 5(12): 379-396, ISSN 1991-8178, 2011.
6. Margo P., M. Heri P., M. Ashari, Hendrik M. and T. Hiyama, "Compensation of Balanced and Unbalanced Voltage Sags using Dynamic Voltage Restorer Based on Fuzzy Polar Control," International Journal of Applied Engineering Research, ISSN 0973-4562 Volume 3, Number 3, pp. 879–890, 2008.

International Journal of Innovations in Engineering and Technology (IJIET)
http://dx.doi.org/10.21172/ijiet.162.02

Cloud Consistency Maintaining As A Service Model For Auditing

KrishnaRao Patwari, T Shravan Kumar
Assistant Professor, Department of Computer Science and Engineering
Avanthi Institute Of Engineering And Technology, Hyderabad, Telangana, India

Abstract- Cloud storage services have become commercially popular due to their overwhelming advantages. To provide ubiquitous always-on access, a cloud service provider (CSP) maintains multiple replicas for each piece of data on geographically distributed servers. A key problem of using the replication technique in clouds is that it is very expensive to achieve strong consistency on a worldwide scale. In this paper, we first present a novel consistency as a service (CaaS) model, which consists of a large data cloud and multiple small audit clouds. In the CaaS model, a data cloud is maintained by a CSP, and a group of users that constitute an audit cloud can verify whether the data cloud provides the promised level of consistency or not. We propose a two-level auditing architecture, which only requires a loosely synchronized clock in the audit cloud. Then, we design algorithms to quantify the severity of violations with two metrics: the commonality of violations, and the staleness of the value of a read. Finally, we devise a heuristic auditing strategy (HAS) to reveal as many violations as possible. Extensive experiments were performed using a combination of simulations and a real cloud deployment to validate HAS.

Keywords – cloud service provider, consistency as a service, heuristic auditing strategy (HAS), consistency as a service (CaaS) model, Platform-as-a-Service (PaaS), Scalability, Security, Local Consistency Auditing, Global Consistency Auditing, logical vector, and physical vector.

I. INTRODUCTION

The Cloud computing is the use of computing resources (hardware and software) that are delivered as a service over a network (typically the Internet). The name comes from the common use of a cloud-shaped symbol as an abstraction for the complex infrastructure it contains in system diagrams. Cloud computing entrusts remote services with a user's data, software and computation. Cloud computing consists of hardware and software resources made available on the Internet as managed third-party services. These services typically provide access to advanced software Applications and high-end networks of server computers.

How Cloud Computing Works-The goal of cloud computing is to apply traditional supercomputing, or high-performance computing power, normally used by military and research facilities, to perform tens of trillions of computations per second, in consumer-oriented applications such as financial portfolios, to deliver personalized information, to provide data storage or to power large, immersive computer games. The cloud computing uses networks of large groups of servers typically running low-cost consumer PC technology with specialized connections to spread data-processing chores across them. This shared IT infrastructure contains large pools of systems that are linked together. Often, virtualization techniques are used to maximize the power of cloud computing.

Characteristics and Services Models: The salient characteristics of cloud computing based on the definitions provided by the National Institute of Standards and Terminology (NIST) are outlined below. **On-demand self-service**: A consumer can unilaterally provision computing capabilities, such as server time and network storage, as needed automatically without requiring human interaction with each service's provider. **Broad network access**: Capabilities are available over the network and accessed through standard mechanisms that promote use by heterogeneous thin or thick client platforms (e.g., mobile phones, laptops, and PDAs). **Resource pooling**: The provider's computing resources are pooled to serve multiple consumers using a multi-tenant model, with different physical and virtual resources dynamically assigned and reassigned according to consumer demand. There is a sense of location-independence in that the customer generally has no control or knowledge over the exact location of the provided resources but may be able to specify location at a higher level of abstraction (e.g., country, state, or data center). Examples of resources include storage, processing, memory, network bandwidth, and virtual machines.

Rapid elasticity: Capabilities can be rapidly and elastically provisioned, in some cases automatically, to quickly scale out and rapidly released to quickly scale in. To the consumer, the capabilities available for

provisioning often appear to be unlimited and can be purchased in any quantity at any time. **Measured service**: Cloud systems automatically control and optimize resource use by leveraging a metering capability at some level of abstraction appropriate to the type of service (e.g., storage, processing, bandwidth, and active user accounts). Resource usage can be managed, controlled, and reported providing transparency for both the provider and consumer of the utilized service.

Services Models: Cloud Computing comprises three different service models, namely Infrastructure-as-a-Service (IaaS), Platform-as-a-Service (PaaS), and Software-as-a-Service (SaaS). The three service models or layer are completed by an end user layer that encapsulates the end user perspective on cloud services. The model is shown in figure below. If a cloud user accesses services on the infrastructure layer, for instance, she can run her own applications on the resources of a cloud infrastructure and remain responsible for the support, maintenance, and security of these applications herself. If she accesses a service on the application layer, these tasks are normally taken care of by the cloud service provider.

Benefits of cloud computing: Achieve economies of scale – increase volume output or productivity with fewer people. Your cost per unit, project or product plummets. Reduce spending on technology infrastructure-Maintain easy access to your information with minimal upfront spending. Pay as you go (weekly, quarterly or yearly), based on demand. Globalize your workforce on the cheap-People worldwide can access the cloud, provided they have an Internet connection. Streamline processes-Get more work done in less time with less people.

Reduce capital costs- There's no need to spend big money on hardware, software or licensing fees. Improve accessibility-You have access anytime, anywhere, making your life so much easier. Monitor projects more effectively-Stay within budget and ahead of completion cycle times. Less personnel training is needed-It takes fewer people to do more work on a cloud, with a minimal learning curve on hardware and software issues. Minimize licensing new software-Stretch and grow without the need to buy expensive software licenses or programs. Improve flexibility.-You can change direction without serious "people" or "financial" issues at stake.

II. RELATED WORKS

Existing System By using the cloud storage services, the customers can access data stored in a cloud anytime and anywhere using any device, without caring about a large amount of capital investment when deploying the underlying hardware infrastructures. The cloud service provider (CSP) stores data replicas on multiple geographically distributed servers. Where a user can read stale data for a period of time. The domain name system (DNS) is one of the most popular applications that implement eventual consistency. Updates to a name will not be visible immediately, but all clients are ensured to see them eventually. Disadvantages Of Existing System-The replication technique in clouds is that it is very expensive to achieve strong consistency. Hard to verify replica in the data cloud is the latest one or not.

System Module: In the first module, we develop the System Module with User Module, Admin Module, and Auditor Module. In user module, user should register their details and get the secret key for login and user can upload the file regarding the auditing. In user module, the user uploaded files can be stored in cloud database. Auditor can view the file from the database it can be much secured. In admin module admin can view all the user details; user uploads details, and TPA activities regarding the auditing strategy. In auditor module, auditor can do the auditing based on the heuristic auditing strategy. It relates with document verification. Auditor can check the auditing file he can reject or accept the file he can revise the report and check whether it's good or bad. And auditor can give revision report like accept or waiting. If status in accept means user can view the file else status is waiting means user cant view the file.

Quality-of-service for consistency of data geo-replication in cloud computing-Today we are increasingly more dependent on critical data stored in cloud data centers across the world. To deliver high-availability and augmented performance, different replication schemes are used to maintain consistency among replicas. With classical consistency models, performance is necessarily degraded, and thus most highly-scalable cloud data centers sacrifice to some extent consistency in exchange of lower latencies to end-users. More so, those cloud systems blindly allow stale data to exist for some constant period of time and disregard the semantics and importance data might have, which undoubtedly can be used to gear consistency more wisely, combining stronger and weaker levels of consistency. To tackle this inherent and well-studied trade-off between availability and consistency, we propose the use of VFC 3, a novel consistency model for replicated data across data centers with framework and library support to enforce increasing degrees of consistency for different types of data (based on their semantics). It targets cloud tabular data stores, offering rationalization of resources (especially bandwidth) and improvement of QoS (performance, latency and availability), by providing strong consistency where it matters most and relaxing on less critical classes or items of data.

Data consistency properties and the trade-offs in commercial cloud storages-The consumers' perspective-A new class of data storage systems, called NoSQL (Not Only SQL), have emerged to complement traditional database systems, with rejection of general ACID transactions as one common feature. Different platforms, and indeed different primitives within one NoSQL platform, can offer various consistency properties, from Eventual Consistency to single-entity ACID.

III. SYSTEM ARCHITECTURE

In System Architecture the System Module with User Module, Admin Module, and Auditor Module. In user module, user should register their details and get the secret key for login and user can upload the file regarding the auditing.

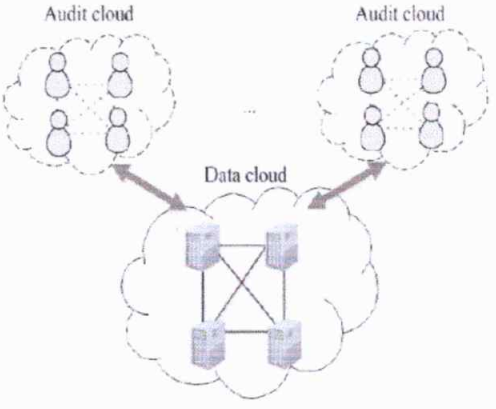


Figure 1. System Architecture

In user module, the user uploaded files can be stored in cloud database. Auditor can view the file from the database it can be much secured. In admin module admin can view all the user details; user uploads details, and TPA activities regarding the auditing strategy. In auditor module, auditor can do the auditing based on the heuristic auditing strategy. It relates with document verification. Auditor can check the auditing file he can reject or accept the file he can revise the report and check whether it's good or bad..If status in accept means user can view the file else status is waiting means user cant view the file. Provide extendibility and specialization mechanisms to extend the core concepts. Be independent of particular programming languages and development process. Provide a formal basis for understanding the modeling language. Encourage the growth of Object Oriented tools market. Support higher level development concepts such as collaborations, frameworks, patterns and components. Integrate best practices. **Image Classification:** In use case diagram, its purpose is to present a graphical overview of the functionality provided by a system in terms of actors, their goals (represented as use cases), and any dependencies between those use cases. The main purpose of a use case diagram is to show what system functions are performed for which actor. Roles of the actors in the system can be depicted .Class diagram in a type of static structure diagram that describes the structure of a system by showing the system's classes, their attributes, operations (or methods), and the relationships among the classes. It explains which class contains information. Sequence diagram is a kind of interaction diagram that shows how processes operate with one another and in what order. It is a construct of a Message Sequence Chart. Sequence diagrams are sometimes called event and timing diagrams, event scenarios.

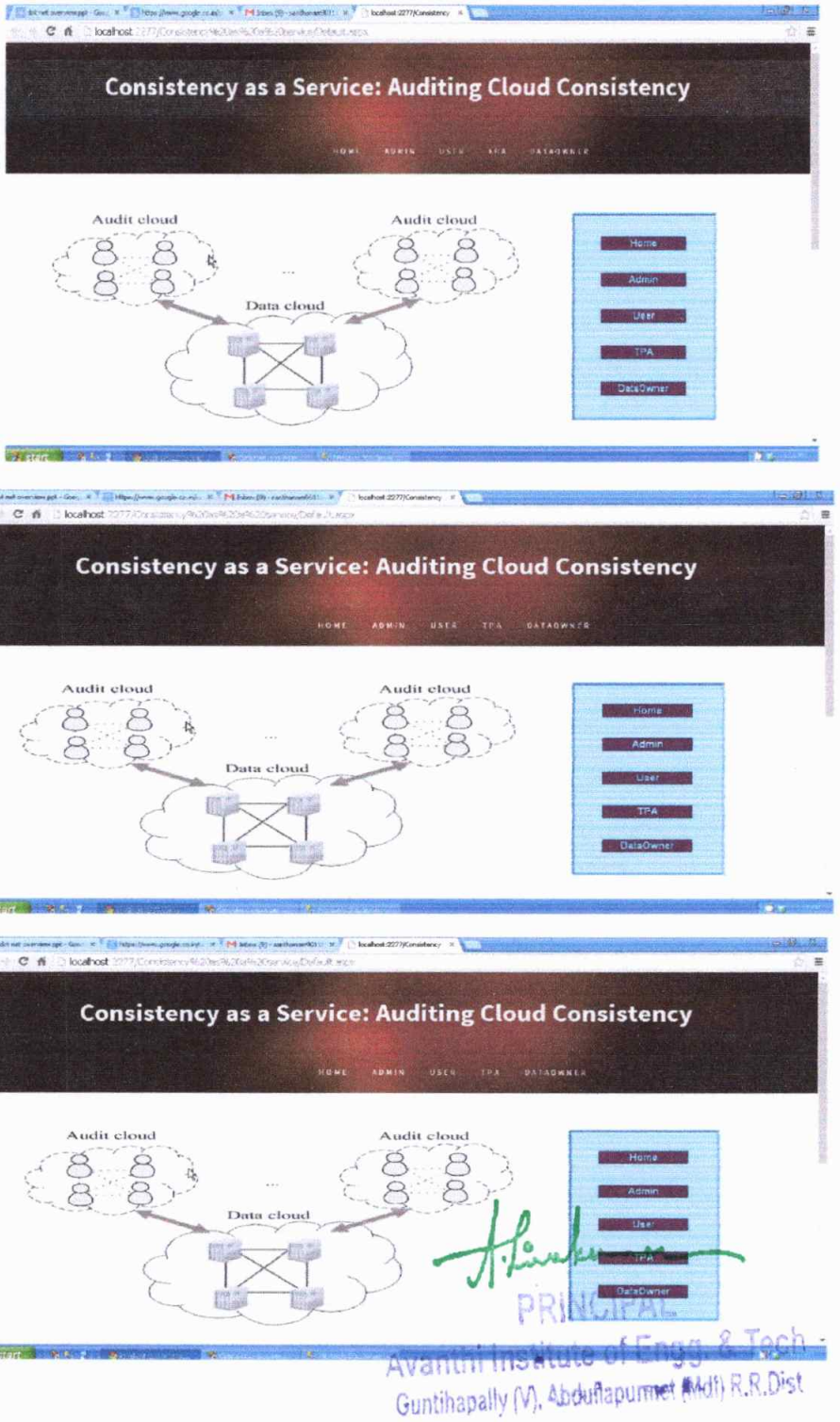
IV. IMPLEMENTATION AND ANALYSIS

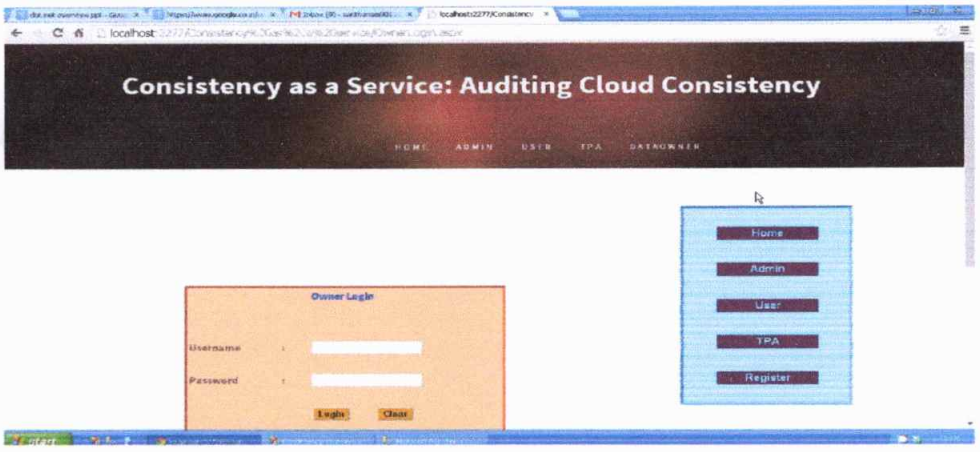
The consistency as a service (CaaS) model and a two-level auditing structure to help users verify whether the cloud service provider (CSP) is providing the promised consistency implemented using Microsoft .NET and C#.. To quantify the severity of the violations, if any. With the CaaS model, the users can assess the quality of cloud services and choose a right CSP among various candidates, e.g., the least expensive one that still provides adequate

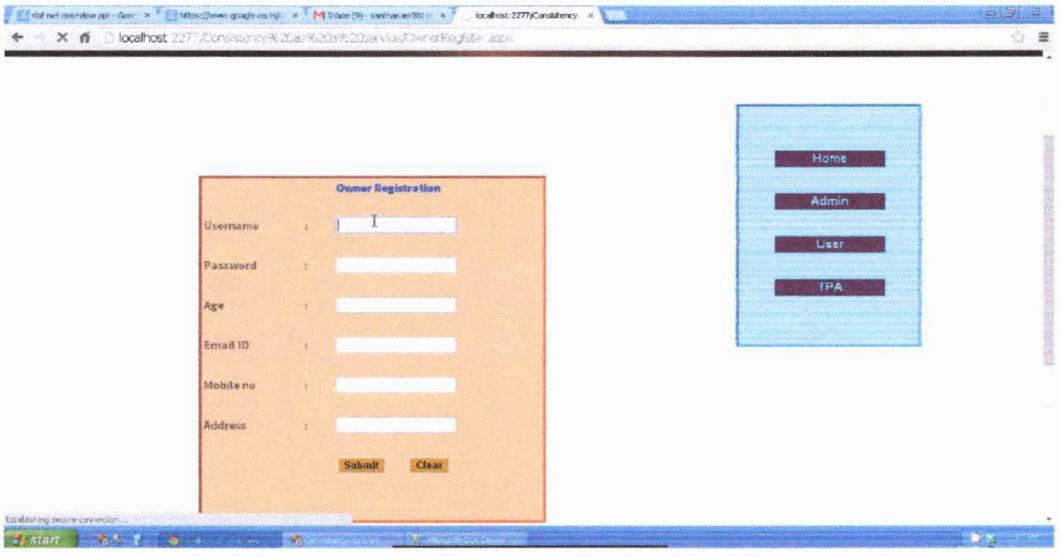
http://dx.doi.org/10.21172/ijiet.162.02

consistency for the users' applications._Advantages of Proposed System-Do not require a global clock among all users for total ordering of operations._The users can assess the quality of cloud services. choose a right CSP._Among various candidates, e.g, the least expensive one that still provides adequate consistency for the users applications.

V. RESULTS







VI . CONCLUSION

A quality output is one, which meets the requirements of the end user and presents the information clearly. In any system results of processing are communicated to the users and to other system through outputs. In output design it is determined how the information is to be displaced for immediate need and also the hard copy output. It is the most important and direct source information to the user. Efficient and intelligent output design improves the system's relationship to help user decision-making.

REFERENCES

[1] M. Armbrust, A. Fox, R. Griffith, A. Joseph, R. Katz, A. Konwinski, G. Lee, D. Patterson, A. Rabkin, I. Stoica, *et al.*, "A view of cloud Computing," *Commun. ACM*, vol. 53, no. 4, 2010.

[2] P. Mell and T. Grance, "The NIST definition of cloud computing (draft)," NIST Special Publication 800-145 (Draft), 2011.

[3] M. Ahamad, G. Neiger, J. Burns, P. Kohli, and P. Hutto, "Causal memory: definitions, implementation, and programming," *Distributed Computing*, vol. 9, no. 1, 1995.

[4] W. Lloyd, M. Freedman, M. Kaminsky, and D. Andersen, "Don't settle for eventual: scalable causal consistency for wide-area storage with COPS," in *Proc. 2011 ACM SOSP*.

[5] E. Anderson, X. Li, M. Shah, J. Tucek, and J. Wylie, "What consistency does your key-value store actually provide," in *Proc. 2010 USENIX HotDep*.

[6] T. Kraska, M. Hentschel, G. Alonso, and D. Kossmann, "Consistency rationing in the cloud: pay only when it Matters," in *Proc. 2009 VLDB.*

[7] S. Esteves, J. Silva, and L. Veiga, "Quality-of- service for consistency of data geo-replication in cloud computing," *Euro-Par 2012 Parallel Processing*, vol. 7484, 2012.

[8] S. Esteves, J. Silva, and L. Veiga, "Quality-of- service for consistency of data geo-replication in cloud computing," *Euro-Par 2012 Parallel Processing*, vol. 7484, 2012.

2020 International Conference on Computer Communication and Informatics (*ICCCI* -2020), Jan. 22 – 24, 2020, Coimbatore, INDIA

Rule-based Mining of Juvenile Delinquency

Lalitha Saroja Thota
Koppula Shireesha, Alla Sravani
S.Rajender
Dept of Computer Science and Engineering,
Avanthi Institute of Engineering & Technology,
Hyderabad, India

Suresh Babu Changalasetty,
Ahmed Said Badawy,
Abdelmoty M.Ahmed,
Wade Ghribi,
Harun Bangali
College of Computer Science,
King Khalid University,
Abha, Saudi Arabia

Abstract— **The incremental expansion of juvenile delinquency or criminal offence done by children below 18 years age is extensively perceived in India. There are innumerable elements like family & parents, schooling & education levels, monetary problems, internet, easy online videos availability, peer groups, mental issues, drugs, media, etc tender for immoral ideas in the teens. In this research paper, we extend the work of association rule mining of Juvenile delinquency [3] with two major risk elements, family background & education levels of children convoluted in crimes. We discover strong rules connecting family background, education levels and juvenile delinquency with Indian Juvenile crime dataset by association rule mining, a rule-based machine learning mechanism**

Keywords-Juvenile delinquency, Data mining, machine learning, Association rule mining, Support, Confidence, WEKA tool

I. INTRODUCTION

The incremental expansion of juvenile delinquency or criminal offence done by children below 18 years age is extensively perceived in India. The recent Hyderabad Disha rape case and Delhi Nirbhaya rape case are few of heinous crimes which persisted long in peoples mind and media. Shockingly some minor childrens are convoluted in these crimes. In 2015 year alone, over 31000 juvenile cases are filed in India as per statistics of National Crime Records Bureau NCRB India [1]. Fig 1 gives graphical overview of the major juveniles crime cases statistics for the years 2010-15 in India.

The soft children mind can be carved and turned towards crimes by innumerable elements like family & parents, schooling & education levels, monetary problems, internet, easy online videos availability, peer groups, mental issues, drugs, media, etc [2]. Family is the learning center for children to learn bad or good qualities. The rejected children by parents or children living with guardians or homeless children are found at high risk of becoming offenders. In building the personality of youth, school education also plays a pivotal role. Some key elements in the schooling setup like expulsions, failures in academics, disciplinary punishments and school dropout also adds juvenile offence cases.

In this research paper, we extend the work of association rule mining of Juvenile delinquency [3] with two major risk elements, family background & education levels of children convoluted in crimes. We discover strong rules connecting family background, education levels and Juvenile delinquency with Indian Juvenile crime dataset by association rule mining, a rule-based machine learning mechanism

II. RELATED WORK

The primitive growth hubs of children are family and home. The family and the parents are primarily responsible for overall development of children and protect them towards negative criminal moments. If a family does not provide support and guidance, the children tend towards crimes.

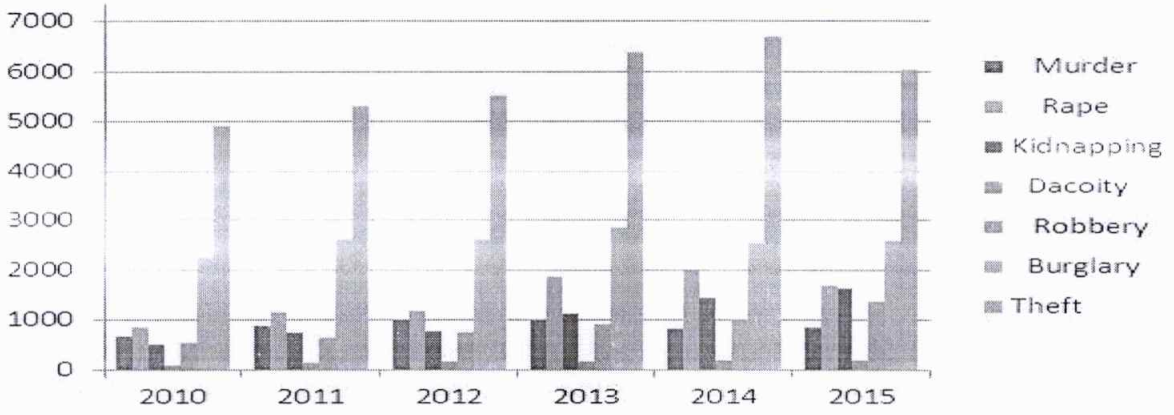


Figure 1 Major Juvenile crimes statistics of India during 2010-15

978-1-7281-4514-3/20/$31.00 ©2020 IEEE

The primary risk elements regarding the family which motivate juvenile crimes are low parent monitoring levels, hard strictness of parents like rude punishments, breakup cases of parents, quarrels & clashes between family members, criminal parents, brothers or sisters etc. [3]. School education is a foundation component in childs life. In school-to-prison pipeline the primary parts found are school suspensions, punishments, academics failures and dropouts. Schept et al [4] reports that crime offending nature in children who dropout schools are eight times more when compared to children passing high school.

Several classification and clustering techniques available in data mining were employed for crime identification, detection and analysis [5,6]. In this research paper, we extend the work of association rule mining of Juvenile delinquency [3] with two major risk elements, family background & education levels of children involved in crimes to discover strong rules in Juvenile delinquency dataset of India

III. METHODOLOGY

Valuable knowledge and information are hidden in large databases and data warehouses. Mining hidden knowledge with various algorithms and methods is data mining process. Few techniques of data mining used in hidden knowledge extraction are generalization, association, classification, clustering etc. which use different algorithms and methods of machine learning. In many fields like banks, insurance, sales & marketing, manufacturing, CRM, health care, bioinformatics, crime analysis and fraud identification etc data mining is used as a powerful tool [7] for beneficial explorations.

Association rule mining [8] is a rule-based machine learning mechanism to discover rules, associations and relations, frequent patterns among key attributes in large warehouses and databases by applying key measures like support, confidence. Rules of association mining are generally like if/then relation having two parts, (if) an antecedent part and (then) a consequent part. The rule form:

Antecedent → Consequent [support, confidence]

An association mining rule example is like:

buys(x,"tea") ^ buys(x,"sugar") → buys(x,"milk") [65%, 95%]

The juvenile crime dataset is built from the overall crime statistics of India [1]. The dataset is loaded in WEKA tool and preprocessing steps are applied. The clean juvenile data is deployed for association mining task to generate association rules which meet minimum support level (65%) and minimum confidence (95%) levels specified by the user. The association rules generated are investigated and appraisal is made for making inferences and interconnections between juvenile crimes and two major risk elements, family background and education levels. An overview of the association rule mining architecture employed with juvenile dataset is shown in Fig 2.

Java an object oriented programming language was used to build WEKA data mining tool. WEKA stands for Waikato Environment for Knowledge Analysis. WEKA software was created by University of Waikato in New Zealand. Several algorithms, methods of machine learning are implemented in WEKA for data preprocessing, association, classification, clustering etc. Huge data can be seen graphically in WEKA with in-built visualization functions [9]

IV. EXPERIMENTS, RESULTS AND DISCUSSIONS

In this research paper we extend the work of association rule mining of Juvenile delinquency [3] with two major risk elements, family background & education levels of children involved in crimes. The juvenile crime dataset is built from the NCRB statistics of India [1]. The crime data contains many crime statistics for years 2001-15. Juvenile crime records (527) are collected by applying filter on the crime data and save in excel sheet. The juvenile crime data of India (part) for years 2001-15 is presented in Fig 3

Excel juvenile data file is saved in CSV format and used in WEKA tool for further processing. In preprocessing stage, we load CSV file and remove unnecessary attributes (area, year, sub group) and discretize some attributes (education level attributes illiterate, upto primary, above primary but below matric, matric or above, family background attributes homeless, living with parents living with guardian and total crime) and prepare the juvenile dataset for association rule mining task. After preprocessing stages, the CSV file is saved in ARFF format. Association rules mining task is applied on the dataset in juvenile ARFF file with apriori algorithm and parameters min support (65%), min confidence (95%) and the five top rules are generated. The WEKA output file with association rules are presented in Fig 4 which shows the co-relating rules of childrens family background & education levels and juvenile crimes.

The top five rules generated with juvenile family background and education levels combined with crimes discovers more illiterate juvenile's are in first category to make crimes. The children who live guardians are in second group youth incline to crimes. The children who study upto primary school are in third tier youth to offend juvenile crimes. Similarly on investigating the fourth and fifth top rules we derive youth who finish metric and above education are in fourth level and juveniles who lives with parents are in fifth zone are making juvenile crimes. We discover strong rules connecting family background, education levels and Juvenile delinquency with Indian Juvenile crime dataset by association rule mining, a rule-based machine learning method

The crime reports and analysis of data in 2015 by NCRB India [1] shows 86% of the apprehended children lived with parents and one third of total juvenile crimes are offended by minors study only upto primary school. The outcome association rules generated in the experiment are similar and in line of the overall NCRB crime statistics of India [1].

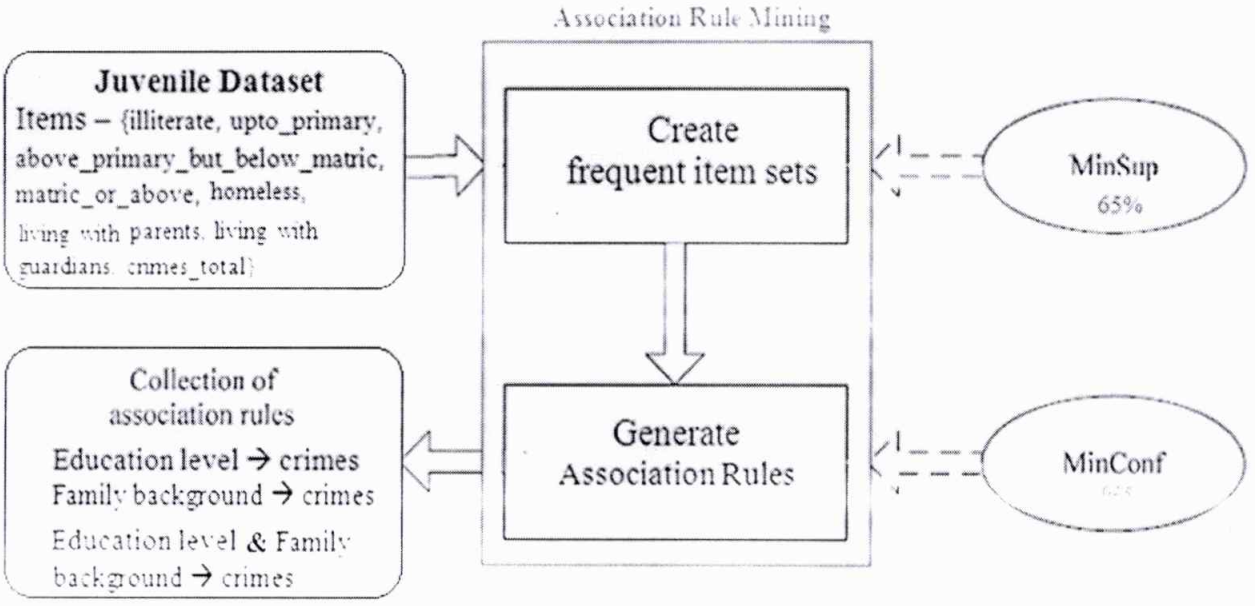


Figure 2. Association rule mining of Juvenile dataset

	A	B	C	D	E	F	G
1	area_name	year	sub_group_na	illiterate	upto_primary	above_primary_but _below_matric	above_matric_or_higher
2	Andaman & Nicobar	2001	1. Education	0	4	12	0
3	Andhra Pradesh	2001	1. Education	640	683	178	64
4	Arunachal Pradesh	2001	1. Education	16	70	39	12
5	Assam	2001	1. Education	91	88	74	0
6	Bihar	2001	1. Education	190	253	87	56
7	Chandigarh	2001	1. Education	12	26	33	0
8	Chhattisgarh	2001	1. Education	205	748	348	61
9	Dadra & Nagar Have	2001	1. Education	0	2	0	0
10	Daman & Diu	2001	1. Education	2	0	0	0

	A	B	C	D	E	F	G
1	area_name	year	sub_group_name	homeless	living_with_parents	living_with_guardian	total_crime
2	Andaman & Nicobar	2001	3. Family Background	0	16	0	16
3	Andhra Pradesh	2001	3. Family Background	552	726	287	1565
4	Arunachal Pradesh	2001	3. Family Background	0	79	58	137
5	Assam	2001	3. Family Background	21	158	74	253
6	Bihar	2001	3. Family Background	43	442	101	586
7	Chandigarh	2001	3. Family Background	0	67	4	71
8	Chhattisgarh	2001	3. Family Background	37	1182	143	1362
9	Dadra & Nagar Have	2001	3. Family Background	0	2	0	2

Figure 3. Juvenile crime data (part) of India during 2010-15

```
=== Run information ===
Scheme:     weka.associations.Apriori -N 10 -T 0 -C 0.9 -D 0.05 -U 1.0 -M 0.1 -S -1.0 -c -1
Relation:   juv5-weka.filters.unsupervised.attribute.Remove-R1-2-weka.filters.unsupervised.attribute.Discretize-B2-M-1.0-Rfirst-last-
precision6-unset-class-temporarily
Instances:  211
Attributes: 8
            illiterate
            upto primary
            above primary but below matric
            matric & above
            living with parents
            living with guardians
            homeless
            total crime
=== Associator model (full training set) ===
Apriori
=======
1. illiterate=0_242 151 ==> total crime=0_4006 151    <conf:(1)> lift:(1.09) lev:(0.06) [12] conv:(12.17)
2. living with guardians=0_175 150 ==> total crime=0_4006 150    <conf:(1)> lift:(1.09) lev:(0.06) [12] conv:(12.09)
3. upto primary=0_436 149 ==> total crime=0_4006 149    <conf:(1)> lift:(1.09) lev:(0.06) [12] conv:(12)
4. matric & above=0_144 149 ==> total crime=0_4006 149    <conf:(1)> lift:(1.09) lev:(0.06) [12] conv:(12)
5. living with parents='(-inf-0.5]' 147 ==> total crime=0_4006 147    <conf:(1)> lift:(1.09) lev:(0.06) [11] conv:(11.84)
```

Figure 4. WEKA output file and association rules relating Education levels & Family background of Juveniles and total crimes

V. Conclusion And Future Work

We examine and analyze the connection of family background & education level risk elements which primarily cause juvenile delinquency with an experimental study with Indian juvenile crime dataset. The results show a strong association of family background & education levels and juvenile delinquency. The association rules generated are similar and in line with India NCRB crime statistics.

In future, studies like this can be undertaken for evaluating many risk elements with distinct algorithms and techniques of machine learning to investigate the connection between all primary risk elements and juvenile delinquency

References

[1] National Crime Records Bureau NCRB India and Government of India Ministry of statistics and programme implementation, Crime - Statistical Year Book India, 2017

[2] Graham J. and Bowling B, Young People and Crime, Home Office Research Study No. 145, London: Home Office, 1995

[3] Suresh Babu Changalasetty, Bouallegue Belgacem, Ahmed Said Badawy, Wade Ghribi, Abdelmoty M.Ahmed, Harun Bangali, Lalitha Saroja Thota, Maroju Shiva Prasad, Rambabu Pemula, Assessing the Relation between Family Background and Juvenile Delinquency using Data Mining, IEEE International Conference on Computer Communication and Informatics (ICCCI), India, Jan 2019

[4] Schept, Wall, Brisman, Judah, Tyler, Avi, Building, Staffing, and Insulating: An Architecture of Criminological Complicity in the School-to-Prison Pipeline, Social Justice, 2015

[5] Wang Peiying, Analysis of the Causes of Juvenile Delinquency Based on the Sociological Angle, IEEE International Conference on Management and Service Science, 2011

[6] Lalitha Saroja Thota, Suresh Babu Changalasetty, et al, Cluster based Zoning of Crime Info, IEEE 2nd International Conference on Anti-Cyber Crimes (ICACC), Abha, Saudi Arabia, March 2017

[7] Suresh Babu Changalasetty, Lalitha Saroja Thota, Ahmed Said Badawy and Wade Ghribi, Classification of Moving Vehicles using K-Means Clustering, IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT-2015), India, Mar 2015

[8] https://en.wikipedia.org/wiki/Association_rule_learning [online],2019

[9] http://www.cs.waikato.ac.nz/ml/weka/ [online], 2019

INTERNATIONAL JOURNAL OF RESEARCH IN EDUCATION AND PSYCHOLOGY (IJREP)
An International Peer Reviewed Journal
http://ijrep.com/
Vol.5 Issue 4
2019
RESEARCH ARTICLE
IJREP Veda Publications
ISSN:2455-426X

PREREQUISITE OF ENGLISH LANGUAGE SKILLS FOR IT RECRUITMENT

Dr.Waheed Shafiah, Mrs. B. Nayeema (Ph.D)

doi: https://doi.org/10.33329/IJREP.2019.48

Abstract

This article throws light on enhancing communication skills through activity based of job recruitment process for B.Tech. Students in St. Ann's College of Engineering and Technology, located at Chirala in Prakasam District. As communication skills are utmost important in one's day today world, there is an urgent need to improve communication Skills in English Language. Most of the B.Tech.students from Prakasam District belong to rural background and their medium of instruction in primary and secondary education is in their mother tongue i.e., in Telugu Language. So, this paper touches with the introduction of their background education, level of understanding and usage of English Language, environment, cultural background. It focuses on the main problems faced at the technical education in B.Tech. Level and at the same time the effective use of innovative techniques or methods used by the Language faculty for performing various tasks like Group Presentations, Inspirational Videos, Role Plays, Group Discussions, Celebrity Interviews, Interview Skills. Developing English language Skills is a prerequisite to acquire employment in a desired multi-national, international and IT sectors. This paper concludes with the appropriate suggestions for acquiring communication skills.

Keywords: *Communication skills in English Language, Recruitment, Group Presentations, Group Discussions, Celebrity Interviews, Inspirational Videos, Critical Thinking and Task based Activities.*

The main aim of engineering students is to acquire a job in a Multinational company or to go for further studies in abroad. For them, effective communication skills are very important besides employability skills. The ability of speaking accurately, appropriately and quickly with a wide variety of people is appreciative. For students both verbal as well as written communication is important which develops professional career and social gathering.

Recruitment Process

Generally, any recruitment process evaluates the candidates in three categories. The first round is conducted on written exam, the second round is on group discussion and the third round is an interview which is sub- divided into two types. They are Technical Interview and Human Resource Interview.

In the first level, the students are tested on written skills which is subdivided into three main divisions i.e., on English, Aptitude and Coding. The topics in English test are on comprehension, vocabulary and on grammar. The aptitude topics are on Arithmetic, logical & analytical reasoning, psychometric test and Coding.

After clearing written examination, the students are eligible for further round that is on Oral performance. The oral test differs from company to company and mostly students are evaluated in Group Discussions or Just a Minute. Though many students clear the written exam, they fail in the second round that is in Group Discussion or Jam. B.Tech. Students need to develop their confidence, ideas, fluency, vocabulary and pronunciation.

The final round of recruitment process is an Interview. Often only one interview is conducted and sometimes two interviews are conducted like Human Resource Interview and Technical Interview. In Human resource interview the candidate is tested in many things like Attitude, Body Language, Fluency, Presence of mind, Fluency, Honesty, Integrity, knowledge & wisdom.

Analyzed a Problem

The first main problem identified is that the B. Tech. students of St. Ann's College of Engineering and Technology are facing many inhibitions like nervousness, fear, hesitation and lack of confidence and poor communication skills in English language. They struggle in framing basic grammatical structures, obstacles in fluency and pronunciation. By digging into the depth of their primary and secondary education, most of students have completed in their education in mother tongue with high percentage and influenced by it. English speaking environment is unknown to them as they hardly listen to English teachers or speeches and their parents are uneducated farmers and weavers. Since their childhood, a sort of fear is indulged in their minds towards English language. When they are asked to speak for a minute in the classroom,

they fail to participate in the activity. When students are forced to speak in the classroom in the next period, they would stop attending the classes with the fear of presenting in English language.

Another major problem identified is that the greater number of periods are allotted for the core subjects of Engineering branches rather than assigning to developing English language teaching. The affiliated university of JNTUK English syllabus is prescribed only in the first year of B. Tech level but not in other three years of B.Tech. life. The last problem is acknowledged is that there is only sufficient number of English faculty in the institution.

Methods / Strategy

There are many methods, strategies and approaches to develop English language. The methods or the strategy applied to the students in campus recruitment training is by giving task-based activities to the students by dividing them in groups. The activities are Group Presentations, Critical Thinking, Inspirational Videos, Group Discussions, Celebrity Interviews, and Mock Interviews.

1.Group Presentations

Group Presentations play a key role in getting confidence to the students. This can be done with SWOT analysis, Just a minute, Public Speeches. First the friendly environment should be created for them then they feel comfortable to speak in English Language.

2. Critical Thinking

Critical Thinking is very important to the student as he/she has to analyze the topic clearly. This can be done by showing them some video Kipling or narrating creative stories.

3. Inspirational Videos

Inspirational videos have lot of influence on the students. It changes them psychologically by listening to the great speeches like Malala Yusufzai, Abdul Kalam,

4.Group Discussions

This is the very important part in the recruitment process. Fluency, ideas, body language, attitude all reflect which discussing the topic. This practice should be done rigorously by the students. Proper evaluation should be given for rectifying their drawbacks.

5.Celebrity Interviews

To make the students more confident and to develop their spontaneity of language, defending skills this activity is conducted by taking the celebrities in education, sports, scientists and politicians. Students with fun easily learn the English language.

6.Mock Interviews

Selection process is not done without interviews. This is the final round of the recruitment. Students are given inputs many mock interviews should be conducted until they become perfect. This helps them in gaining subject knowledge as well as confidence.

Solution

1. The best solution is that these above activities that are mentioned in this paper should be continued every day for every year of B.Tech. classes.

2. Minimum Two periods class should be at a stretch.

3. Every Student should be given an opportunity to speak and assessed properly.

4. Friendly environment should be created in the class.

5. Every student should be encouraged by giving a small gift of appreciation.

6. Their Group Discussions or presentations should be recorded for identifying their own mistakes in body language and fluency.

Conclusion

This paper concludes by focusing on the prerequisite of English Language skills for employability. Problems of learners in level of understanding and using of English Language, has improved a lot through the techniques or methods which has applied to develop communication skills. The teacher's role should be only felicitating and students have been more responsible in playing multiple tasks actively. With this observation the analysis found is definitely most of the students become more proficient in using English language in the task-based activities like Group Presentation, Role Plays, Group Discussion, Mock Interviews and Celebrity Interviews. The outcome of the task-based activities is B.Tech. students' performance has improved, enhanced their fluency, became more confident in placing multinational and international companies.

Research Paper
Impact Factor: 6.304
Peer Reviewed & Indexed Journal
www.iibarr.com

IJBARR
E- ISSN -2347-856X
ISSN -2348-0653

INFLUENCE OF ORGANISATIONAL CITIZENSHIP BEHAVIOUR FACTORS ON JOB SATISFACTION AMONG ENGINEERING COLLEGE TEACHERS IN ANDHRA PRADESH

B.Nayeema* Dr.V.Tulasi Das*
**Ph.D. Scholar, Dept. of HRM, Acharya Nagarjuna University, Guntur-522 510, A.P.*
***Associate Professor, Dept. of HRM, Acharya Nagarjuna University, Guntur-522 510, A.P.*

Abstract
In the current scenario, the emergence of many private universities increases the demand for the engineering faculty members and so it's difficult for the management to retain the talented pool. The teaching and learning process will be more effective in an institution where the faculty members are contented with their job. Job satisfaction is the major tool which makes employees contented with their job. University professors are differ in so many ways from other employees, including highly educated professional employees, so there is dailama among research community that university faculty job satisfaction factors are same as other employee job satisfaction. Therefore, the present research focuses on to understand which organisational citizenship behaviour factors are significantly contributing for job satisfaction among Public Sector University Engineering College

Key Words: Job Satisfaction, Organisational Citizenship Behaviour, Talent, Teaching and Learning Process.

Introduction

Organizational citizenship behavior is a extensively discussed concept in the field of organizational behavior and in recent years researchers have paid more attention to these mutual employee behaviors. Organizational Citizenship Behavior (OCB) is a discretionary code of behavioral attributes that goes beyond the basic requirement of the job. In today's competitive global and competitive business world, OCB has happened to a point of importance. Positive OCB has been found to have a significant impact on employee performance. The motivation for choosing OCB as the research ground is its positive relationships with employee performance. By measuring OCB, management can pave the way to increase employee performance.

Organizational citizenship behaviors emerged by multiple factors such as loyalty, helping others, respect, benefits, etc. If an employee possesses OCB he or she will be ready to contribute their efforts and skills to organizations even if it is not officially requested by them. Organizational citizenship behavior is defined as "an individual behavior that is discretionary, not directly or explicitly recognized by the awarded formal system, and which overall promotes the effective functioning of the organization" (Organ, 1990).

The organizational behavior of citizenship supports to optimise the organizational performance of businesses. OCB's plays the role of prime factor in achieving productivity and performance in any business concern. OCB is necessary for the growth, success, effectiveness and productivity of any businessorganization. In Bangladesh, OCB provides superior business performance as follows:

1. Increase collaboration or management performance.
2. Understand human resources knowledge and skills (HR Audit) so that underutilized and unutilized skills and knowledge can be used in more productive domines.
3. Coordinate activities within and between working groups
4. Building Organisational Brand Image so that skilled employees can be attracted and retained.
5. Adopting best Change Management Practices to stability the organization from future environmental changes.

Batman and Organ (1983) for the first time presented the idea of citizenship's organizational behavior. Organ (1988) defined OCB as "Individual behavior that is discretionary, not directly or explicitly recognized by the formal reward system, and which overall promotes the effective functioning of the organization" More attention should be paid to the direction to increase the OCB because the success of the organization and the perception of customers to provide good quality services are significantly correlated with OCB. (Torlak & Koc, 2007).

According to Organ (1988) in OCB an individual's behavior is discretionary. This behavior is not recognized directly or explicitly by the formal reward system and, in general, promotes the effective functioning of the organization. Katz (1964) paid attention to the concept of employee extra-role behavior. Katz noted that employees are willing to contribute to the extra efforts to achieve organizational results. A distinctive feature is that supervisors cannot request or force their subordinates to perform OCBs. Likewise, employees do not expect or cannot expect any form of formal reward for these discretionary behaviors. However, as Organ (1997) observed, supervisors regularly take into account and reward the OCB exhibited by subordinates both directly and indirectly (eg preferential treatment, performance evaluation, promotions, etc.).

One more essential statement, especially in Organ's (1988) foundation work on OCB, is that these behaviors are often motivated internally, deriving from within and supported by an individual's intrinsic need for a sense of accomplishment, competence, membership or affiliation.

Van Dyneet al (1998) proposed the broader construct of "extra-role behavior" (ERB), defined as "behavior for the benefit of the organization and / or intended for the benefit of the organization, which is discretionary and which goes beyond the existing role expectations. " OCB generally refers to behaviors that have a positive impact on the organization or its members (Poncheri, 2006). OCB can be defined as defender of the organization when peers are criticized or urged to invest in the organization (Turnipseed &Rassuli, 2005). The researchers define the OCB in contexts and not very different contexts, moreover there is a lot of coherence in their ways of interpreting the OCB. Jacqueline et al. (2004) indicates that OCB is extra-role behavior, that is, any behavior not officially required by the organization; rather its practice depends solely on the employee's consent as a consequence of the organizational environment. OCB affects the effectiveness of the organization.

The OCB is having a meticulous influence on the overall productivity of organizations by accumulating different dimensions to the social framework of the workplace environment (Todd, 2003). In some cases, the organizational citizenship behaviour is defined as a set of voluntary behaviors (which are not part of employee's job description), which intern lead to a successful enhancement of the roles and responsibilities of the organization (Appelbaum, 2004). Organizational citizenship behavior is observed as an employee's voluntary behavior that leads to the development of the effectiveness and efficiency of the organization's operation (to which it is not officially recorded and rewarded by the organization's established system) (Hall, 2005). Employees' who appreciate this function show behaviors beyond their official roles, duties and details of the job. The main aim for this type of behavior is not earning any organizational reward, but they use all their efforts for the improvement and development of the organization (Taghavi, 2011).

Literature indicates that those employees who act beyond their duties and responsibilities and exhibit organizational citizenship behaviors enjoy superior productivity and quality in their organization and team (Podsakoff, 1997). What is evident is that organisational citizenship behavior cannot be strengthened.

Job Satisfaction and Organisational Citizenship Behaviour

The dominant variable that influences the behavior of organizational citizenship is professional satisfaction (RE Suryani et., Al, 2019). There is a direct relationship or a strong positive correlation between organizational citizenship and professional satisfaction (AH. Shalaby, 2015). Professional satisfaction mediated the relationship between organizational culture and organizational citizenship behavior (Badawy, 2017). The critical roles of job satisfaction components have positive and significant effects on organizational citizenship and Vice Versa (AH. Shalaby, 2015). The employee satisfied with engaging in the OCB (Fassina et al., 2008). When employees are more satisfied, it creates a positive character and ultimately leads to socially accepted behavior (Todo, 2003). Positive organizational behavior is a predictor of professional satisfaction and organizational citizenship behavior (Z Pouramini, M Fayyazi, 2015). There were no significant effects on gender, age, years of experience and education levels on OCB and job satisfaction (Badawy, 2017).

Review of Literature

Azza H. Shalaby (2015), In their article entitled "The Effect of Control Variables of Job Satisfaction and Organizational Citizenship on the Performance of External Auditor (Field Study in Saudi Arabia)" published in *International Journal of Finance and Accounting* found that "there is a Relationship between job satisfaction and job performance would be positive if the organization provides constructiveprospects such as lifelong learning, path to grow and reachpre-designed career path. There is a strong correlation between Organizational Citizenship and job performance based on these variables, recognition and rewards, working conditions, relationship with supervisor teamwork. Job satisfaction and Organizational Citizenship have a positive impact on the job performance of the external auditor on the basis of these values' honesty, trust, respect for others etc".

Rahayu Endang Suryani, et.al., (2019), In their article entitled "Job Satisfaction and Citizenship Behaviour of Employees of Private Universities in the Central Jakarta Region" published in *International Review of Management and Marketing* identified that "There is a significant effect of organizational commitment and work-life balance on Job Satisfaction in accredited University employees in the Central Jakarta region and the dominant variable influential is an organizational commitment (Affective commitment). The dominant variable influencing on the behaviour of organizational citizenship is job satisfaction with the dimensions of working conditions that support".

Tarek A. El Badawy, et. al., (2016), in their article entitled "Exploring the Relationship between Organizational Culture, Job Satisfaction and Organizational Citizenship Behaviour" published *International Journal of Human Resource Studies* showed that "job satisfaction had a significant positive correlation with the overall organizational citizenship behaviour. However, the disaggregation reflected that only altruism, sportsmanship, and civic virtue had significant correlations. Finally, the results showed that job satisfaction mediated the relationship between organizational culture and organizational citizenship behaviour. However, the mediation effect was minor as evident by the small decrease in the B coefficient".

Tarek A. El Badawy, et.al., (2017), in their article entitled "The Demographics' Effects on Organizational Culture, Organizational Citizenship Behaviour and Job Satisfaction: Evidence from Egypt and Mexico" published in *Business and Management Research* suggested that "Managers should be aware of the importance of a strong consistent culture that is easily identifiable. Human resource practitioners inside organizations should search for areas of deficiency in their employee cultural orientations. Managers should also be interested in eliciting advice from their employees (across different age ranges and managerial levels) on what makes them motivated and satisfied and what obstacles are hindering them from performing well. In addition, contextual performance should be monitored and awarded in the right moment to encourage employees to engage in citizenship behaviours that serve the organization".

Zahra Pouramini & Marjan Fayyazi (2015), in their article entitled "The Relationship between Positive Organizational Behaviour with Job Satisfaction, Organizational Citizenship Behaviour, and Employee Engagement" published in *International Business Research*this study adds to the understanding of key-role positive organizational behaviour in organization and work-related performance. It implies that, POB is a significant forecaster of JobSatisfaction and when Positive Organisational Behaviour is high then the relationship also found to be stronger. Likewise, there are positive relationships among POB, OCB and employee engagement and such relationships found to be stronger when the POB was high. Therefore, POB plays a significant role in the organization and it is a strategic tool for gaining competitive advantage.

Research Gap

Very less literature is available OCB impact on job satisfaction and in the education sector the literature available is very nominal. In this context this article focuses on OCB impact on Job Satisfaction among Public Sector University Engineering Teachers.

Research Paper
Impact Factor: 6.304
Peer Reviewed & Indexed Journal
www.iibarr.com

IJBARR
E- ISSN -2347-856X
ISSN -2348-0653

Objectives

- To examine influence of Organisational Citizenship Behaviour factors on Job Satisfaction of the select Public Sector University Engineering College Teachers.
- To put forth certain suggestions based on the findings.

Sample and data collection

A quantitative approach was followed in this exploratory study. The participants selected for this study consisted of engineering college teachers working in Andhra University, Sri Venkateshwara University, JNTU Kakinada, JNTU Anantapur. 180 questionnaires were distributed in the study area. Purposive sampling technique was deployed in sample selection. The respondents were solicited to complete the Organisational Citizenship Behaviour Questionnaire. The resultant response rate of useable questionnaires was 83.3% (150).

Data Analysis and Interpretation:

KMO (Kaiser-Meyer-Olkin) and Bartlett's test

Kaiser-Meyer-Olkin (KMO) test is a measure to check how best suites present data for Factor Analysis. This test measures sampling adequacy for each variable in the model and for the complete model as well. The statistic is a measure of proportion of variance among variance. The lower the proportion, the more suited the data is for Factor Analysis. Following Table- 1 shows the results of the KMO and Bartlett's test.

Table- 1: **KMO and Bartlett's Test Relating to Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers**

KMO and Bartlett's Test		
Kaiser-Meyer-Olkin Measure of Sampling Adequacy.		.911
Bartlett's Test of Sphericity	Approx. Chi-Square	6274.558
	df	190
	Sig.	.000

(Source: Primary Data/ Structured Questionnaire)

The above Table- 1 reveals that KMO value i.e., .911 is neither nearer to zero nor close to one. So, the range is found to be good. Bartlett's test for Sphericity compares correlation matrix (a matrix of Pearson correlation) to the identity matrix. In other words, it checks if there is a redundancy between variables that can be summarized with some factors. Therefore, this test should be momentous (i.e., have a significant value less than 0.05). A significant value from chi-square test shows that for the present data R-matrix is not an identity matrix. Here Bartlett's test for Sphericity is highly significant ($p<0.001$), therefore it is concluded that the factor analysis is appropriate.

Communalities

Initial communalities estimate the differences among each factor accounted for, from all the variables. Extraction communalities values are estimates of the differences in each factor accounted for the variables in the factor solution. Below Table- 2 shows the particulars of communalities of Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers.

Table- 2: Communalities- Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers

Communalities		
	Initial	Extraction
I am willing to assist new colleagues to adjust to the work environment	1.000	.859
I am willing to stand up to protect the reputation of the institution	1.000	.772
I am willing to help colleagues solve work related problems	1.000	.914
I often arrive early and start to work immediately	1.000	.907

I am eager to tell outsiders good news about the institution	1.000	.894
I am willing to coordinate and communicate with colleagues	1.000	.821
I actively attend institution meetings	1.000	.778
I take one's job seriously and rarely make mistakes	1.000	.950
I make constructive suggestions that can improve the operations of the institution	1.000	.947
I am willing to cover work assignment for colleagues when needed	1.000	.877
I comply with the institution rules and procedures even when nobody watches and no evidence can be traced	1.000	.711
I avoid consuming a lot a time complaining about trivial matters	1.000	.935
I do not mind taking on new challenging assignments	1.000	.935
I avoid taking actions that hurt others	1.000	.922
I avoid hurting other people's right to common / shared resources	1.000	.918
I perform only required tasks	1.000	.874
I do not initiate actions before consulting with others that might be affected	1.000	.902
I try to avoid creating problems for colleagues	1.000	.900
I try hard to self – study to increase the quality of work outputs	1.000	.933
I avoid focussing on what's wrong with his or her situation	1.000	.943
Extraction Method: Principal Component Analysis.		

(Source: Primary Data/ Structured Questionnaire)

The above table-2 gives the communalities of initial and extraction. Principal component analysis deals with the initial hypothesis that all factors are common; so, in the table, values for the initial communalities are 1 for all the factors. The value in the column titled extraction shows the common differences in the data structure. For, I take one's job seriously and rarely make mistakes 95.0 percent of variance observed is common difference. There is second dimension for observing these communalities is in terms of the ratio of difference explained by the underlying variables.

To understand about the exact level of difference among factors is initially assumed as all communalities are "1". But after the analysis the differentiated values for each variable are found. assist new colleagues has 85.9 per cent, stand up to protect the reputation of the institution has 77.2 per cent, help colleagues solve work related problems has 91.4 per cent, arrive early and start to work immediately has 90.7 per cent, eager to tell outsiders good news about the institution has 89.4 per cent, coordinate and communicate with colleagues has 82.1 per cent, actively attend institution meetings has 77.8 per cent, make constructive suggestions has 94.7 per cent, cover work assignment for colleagues has 87.7 per cent, comply with the institution rules has 71.1 per cent, avoid consuming a lot a time in complaining has 93.5 per cent, taking on new challenging assignments has 93.5 per cent, avoid taking actions that hurt others has 92.2 per cent, avoid hurting other people has 91.8 per cent, perform only required tasks has 87.4 per cent, do not initiate actions before consulting with others has 90.2 per cent, avoid creating problems for colleagues has 90.0 per cent, try hard to self – study to increase the quality of work outputs has 93.3 per cent, and avoid focussing on what's wrong with his or her situation has 94.3 per cent. Above variables shows the variance in structure. It is shown in Total variance Explained table which is following.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Research Paper
Impact Factor: 6.304
Peer Reviewed & Indexed Journal
www.iibarr.com

IJBARR
E- ISSN -2347-856X
ISSN -2348-0653

Table- 3: Total Variance Explained- Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers

Total Variance Explained

Component	Initial Eigenvalues			Extraction Sums of Squared Loadings			Rotation Sums of Squared Loadings[a]
	Total	% of Variance	Cumulative %	Total	% of Variance	Cumulative %	Total
1	15.121	75.604	75.604	15.121	75.604	75.604	12.683
2	1.561	7.804	83.407	1.561	7.804	83.407	13.227
3	1.010	5.052	88.459	1.010	5.052	88.459	11.874
4	.511	2.554	91.013				
5	.410	2.048	93.061				
6	.284	1.420	94.481				
7	.246	1.231	95.712				
8	.176	.880	96.592				
9	.136	.681	97.273				
10	.111	.554	97.827				
11	.094	.472	98.299				
12	.085	.426	98.726				
13	.077	.385	99.111				
14	.064	.318	99.429				
15	.046	.228	99.657				
16	.029	.147	99.804				
17	.017	.083	99.887				
18	.015	.073	99.959				
19	.008	.038	99.997				
20	.001	.003	100.000				

Extraction Method: Principal Component Analysis.

a. When components are correlated, sums of squared loadings cannot be added to obtain a total variance.

(Source: Primary Data/ Structured Questionnaire)

The above Table- 3 shows that Eigen values related with each factor displays the differences explained by that particular linear factor. This table also shows the Eigen values in terms of percentage of difference explain. So, factor 1 explains 75.604, factor 2 explains 7.804 per cent factor 3 explains 5.502 per cent of total variance; it should be clear that these three factors explain relatively large amount of variance of 88.459. Finally, it is concluded that the initial three variables explain relatively major part of difference whereas subsequent variables explain only small part of difference. There are three variables among all with Eigen value greater than 1. The Eigen values related with these variables are again shown and the percentages of difference explained in the columns are labelled extraction sums of squared loadings.

Form the above table-3 it is identified that only first three factors in Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers are highly impacting aspect and the residual were of not that much. Because it only exceeds Eigen value more than 1.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

Table- 4: Pattern Matrix[a]—Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers

Pattern Matrix[a]			
	Component		
	1	2	3
I make constructive suggestions that can improve the operations of the institution	.992		
I take one's job seriously and rarely make mistakes	.950		
I am willing to cover work assignment for colleagues when needed	.940		
I avoid consuming a lot a time complaining about trivial matters	.876		
I actively attend institution meetings	.803		
I comply with the institution rules and procedures even when nobody watches and no evidence can be traced	.757		
I try hard to self – study to increase the quality of work outputs		-.968	
I do not initiate actions before consulting with others that might be affected		-.966	
I avoid focussing on what's wrong with his or her situation		-.965	
I perform only required tasks		-.938	
I try to avoid creating problems for colleagues		-.933	
I avoid hurting other people's right to common / shared resources		-.871	
I avoid taking actions that hurt others		-.860	
I do not mind taking on new challenging assignments		-.835	
I am eager to tell outsiders good news about the institution			.918
I am willing to help colleagues solve work related problems			.896
I am willing to assist new colleagues to adjust to the work environment			.881
I am willing to coordinate and communicate with colleagues			.836
I often arrive early and start to work immediately			.809
I am willing to stand up to protect the reputation of the institution.			.594
Extraction Method: Principal Component Analysis. Rotation Method: Oblimin with Kaiser Normalization.			
a. Rotation converged in 13 iterations.			

(Source: Primary Data/ Structured Questionnaire)

Above Table- 4 shows the Pattern Matrix[a]- Organisational Citizenship Behaviour Factors in select Public Sector University Engineering colleges. On the basis of Oblimin with Kaiser Normalization, three groups emerged. These three groups consist of all those factors that have factor loadings greater than or least equal to 0.5. Thus, the

first group consist six dimensions and this group is titled as OCB1. For second component there are eight dimensions and these eight dimensions are combined together to get one group extracted and it is conceptualized as OCB2. For third component there are six dimensions and these eight dimensions are combined together to get one group extracted and it is conceptualized as OCB3. These three groups are considered for further study.

Table- 5: Component Correlation Matrix- Organisational Citizenship Behaviour among Public Sector University Engineering College Teachers

Component Correlation Matrix			
Component	1	2	3
1	1.000	-.743	.747
2	-.743	1.000	-.703
3	.747	-.703	1.000
Extraction Method: Principal Component Analysis. Rotation Method: Oblimin with Kaiser Normalization.			

(Source: Primary Data/ Structured Questionnaire)

The final part of the factor analysis output is a component Correlation matrix between the factors. This matrix contains the correlation coefficients between the factors. From Table- 5 it is understood that all these factors are interrelated with each other to some degree. The fact that these correlations exists tells that the constructs measured can be interrelated. If the constructs are independent then the component correlation matrix should have been identity matrix. Therefore, from this final matrix it appears that the independence of the factors cannot be assumed.

Findings

1. From the analysis it is found that for Job Satisfaction total 20 Organisational Citizenship Behaviour factors found to be significant.
2. From the patten matrix table it is observed that 20 factors are classified into three groups.
3. "I make constructive suggestions that can improve the operations of the institution" is found to be highly significant.
4. "I am willing to stand up to protect the reputation of the institution" found to be less significant.

Suggestions

1. From the analysis it is observed those faculties are ready to improve the quality of the institution. Universities should form Quality Circles and faculty members should be given a chance to give suggestions for the development of the department as well as institution.
2. Faculty are interested in improving their knowledge and enhancing their teaching skills, but the university schedules are very tight faculty hardly gets time for improving knowledge and AICTE again asking them to attend online courses, seminars and contribute to research ass well so it is creating pressure among the faculty. Therefore, AICTE should give guides lines are maximum hours of teaching by one faculty in a week keeping all afore said development activities in mind.

Conclusion

The present research is conducted to understand which OCB factors are significantly contributing for job satisfaction in select Public sector University Engineering College in Andhra Pradesh.Samanvitha Swaminathan & David Jawahar (2013) 20-point scale of OCB is adopted for the study. After the study it is understood that all 20 factors of OCB are significantly contributing for the Job Satisfaction in the study area. Therefore, policy makers should keep all the 20 factors in mind while ensuring Job satisfaction of their employees (precisely engineeringfaculty).

Scope for Further Study

In future researchers can consider a greater number of faculty as well as institutions for the study to get better picture of the relation. Researcher can identify mediators of OCB and Job satisfaction so that changes in Job satisfaction can be seen with magnifying glasses.

References

1. Appelbaum, S., Bartolomucci, N., Beaumier, E., Boulanger, J., Carrigan, R., Dore, I., Girard, C., and Serroni, C. (2004), "Organizational citizenship behavior:A case study of culture, Leadership and trust", Management Decision, Vol 42 No1, pp.3-40.
2. Azza H. Shalaby (2015). The Effect of Control Variables of Job Satisfaction and Organizational Citizenship on the Performance of External Auditor (Field Study in Saudi Arabia). International Journal of Finance and Accounting, 4(6), Pp: 311-323
3. Batman TS, Organ, DW (1983) Job satisfaction and the good soldier: The relationship between affect and employeecitizenship, Academy of Management Journal 26: 587-595.
4. Fassina, NE, Jones DA and Uggerslev KL (2008) Meta-analytic tests of relationships between organizational justice and organizational citizenship behavior: testing agent-system and shared-variance models. Journal of Organizational Behavior. 29: 805-828.
5. Hall E., Altman M., Nuko N., Peltzer K., & Zuma K. (2005). Potential Attrition inEducation: the Impact of Job Satisfaction, Morale, Workload and HIV/AIDS
6. Jacqueline, A-M.,Shapiro, C., Kessler, I., & Purcell, J. (2004). Exploring Organizationally Directed Citizenship Behaviour: Reciprocity or 'It's my job'? Journal of Management Studies, Vol. 41, pp. 1.
7. Katz D(1964) The motivational basis of organizational behavior. Behavioral Science. 9 (2): 131-146.
8. Laura M. Desimone, Andrew C. Porter, Michael S. Garet, Kwang Suk Yoon and Beatrice F. Birman (2002). Effects of Professional Development on Teachers' Instruction: Results from a Three-Year Longitudinal Study. Educational Evaluation and Policy Analysis, Vol. 24, No. 2 (Summer, 2002), pp. 81-112
9. Linn Van Dyne and Jeffrey A. LePine (1998). Helping and Voice Extra-Role Behaviors: Evidence of Construct and Predictive Validity. The Academy of Management Journal, Vol. 41, No. 1 (Feb., 1998), pp. 108-119.
10. Meyer, J. P., Allen, N. J., & Smith, C. A. (1993). Commitment to organizations and occupations: Extension and test of a three-component conceptualization. Journal of applied psychology, 78(4), 538.
11. Moorman RH (1991) Relationship between organizational justice and organizational citizenship behaviors: Do fairness perception influence employee citizenship? Journal of Applied Psychology.76(6): 845-855.
12. Organ, D W (1988) A restatement of the satisfaction-performance hypothesis.Journal of Management. 14:547-557.
13. Organ, D.W. (1997), "Organization Citizenship Behaviour: It's construct Clean-Up Time", Human Performance, Vol 10 No2, pp. 85-97.
14. Organ, DW (1990) The motivational basis of organizational citizenship behaviour. In: B. M. Staw & L. L. Cummings (eds.) Research in organizational behaviour. Greenwich, CT: JAI, pp. 43-72.
15. Podsakoff, P.M., Ahearne, M., and MacKenzie, S.B. (1997), "Organization Citizenship Behaviour and the Quantity and Quality of Work group Performance", Journal of Applied Psychology, Vol 82, pp.262-70.
16. Poncheri, R. (2006). The Impact of Work Context on the Prediction of Employee Performance. North Carolina State University. Pond, S., Nacoste.
17. Rahayu Endang Suryani, Herminda, Darmin (2019). Job Satisfaction and Citizenship Behavior of Employees of Private Universities in the Central Jakarta Region. International Review of Management and Marketing, 9(2), 54-56.
18. Samanvitha Swaminathan & David Jawahar (2013). Job Satisfaction as A Predictor of Organizational Citizenship Behavior: An Empirical Study. Global Journal of Business Research, Vol 7, No 1, Pp: 71- 80.

19. Tarek A. El Badawy, Juana Cecilia Trujillo-Reyes& Mariam M. Magdy (2017). The Demographics' Effects on Organizational Culture, Organizational Citizenship Behavior and Job Satisfaction: Evidence from Egypt and Mexico. Business and Management Research, Vol. 6, No. 1, Pp: 28- 41.
20. Todo SY (2003) A causal model depiction the influence of selected task and employee variables on organizational citizenship behavior. Unpublished PhD Thesis, The Florida State University, CA. USA.
21. Torlak, O., and Koc, U. (2007), "Materialistic attitude as an antecedent of organizational citizenship behaviour", Management Research News,Vol 30 No 8, pp.581-596.
22. Turnipseed, D. L., & Rassuli, A. (2005). Performance Perceptions of Organizational Citizenship Behaviours at Work: A Bi-Level Study among Managers and Employees. British Journal of Management, 16(3), 231–244.
23. Zahra Pouramini & Marjan Fayyazi (2015). The Relationship between Positive Organizational Behaviour with Job Satisfaction, Organizational Citizenship Behaviour, and Employee Engagement. International Business Research; Vol. 8, No. 9, Pp: 57- 66.

INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY
ISSN [O]: 2582-1431 VOLUME-II ISSUE-II APR-JUNE-2020

Design of Hybrid Energy Storage Systems in DC Microgrid Applications

M.Ragini
Asst.Professor in Department of EEE,Avanthi institute of engineering & Technology(JNTUH).
Email: raginibtech236@gmail.com
Shaikh Mustak Suban
PG Student in Department of EEE,Avanthi institute of engineering & Technology(JNTUH).
Email: mustakshaikh9489@gmail.com

***Abstract*—Due to smooth integration with renewable power resources in addition to the proliferation of dc-well suited loads, dc microgrids are gaining recognition. Because of the excessive penetration of renewable strength sources in dc microgrids, those microgrids are relatively vulnerable to fluctuations in the electricity era. It is harmful, so extreme voltage balance is considered. To absorb these fluctuations within, a battery-primarily based electricity storage gadget and hybrid energy storage machine (HESS), including a battery and supercapacitor (SC), are proposed. The specific traits of the cell and supercapacitors cause them to a super aggregate for HESS applications. The HESS is interfaced with dc microgrid using a double-enter bidirectional converter. This bidirectional converter gives decoupled manipulate of battery and supercapacitor power. This thesis provides a converter modeling technique for the double-input bidirectional converter. A controller was designed based totally in this for voltage law utility for a dc microgrid. The operation of the converter made it feasible to use the equal controller for each HESS charging and discharging process, consequently making it a unified controller. The designed controller was also capable of reject disturbances from the source facet in addition to load facet even as keeping the voltage balance of the dc microgrid. Operation of the converters and overall performance of the designed controller in voltage stability was tested with simulation consequences for each battery by myself garage gadget and hybrid power storage systems.**

***Index Terms*—microgrid, battery, hybrid energy storage machine, controller.**

I. INTRODUCTION

As fossil fuels are diminishing; therefore, there is a demand for renewable energy sources has been increased in the power sector. Also, due to the usage of fossil fuels, there is a lot of impact on the environment. To avoid environmental pollution gradually, we are switching towards renewable energy sources, while solar energy has higher demand amongst other renewable energy sources. As there is a lot of research is going on, solar energy storage and DC-DC converters, the DC microgrid becoming popular nowadays. The room of solar energy became more comfortable and more efficient and reutilizing the storage energy by using a DC-DC converter, whenever their deficiency of power at the grid. Furthermore, the integration of the electrical storage system also improves the reliability of the power system.

A. DC-DC Converter Control Schemes

DC-DC converters are very widely used in many applications such as microgrid, smart grid, plug-in hybrid electric vehicles, etc. The boost converter is non-linear and has a non- minimum phase structure due to the presence of right half zero. Disturbances present in the source side or load side also affects the system. So, it is required to control the output voltage and reducing the steady-state error. Several linear and non-linear, analog and digital control techniques are already designed, each having its own set of advantages and disadvantages. The classical control technique uses the state-space averaging method and linearization of non-linear system equations around the equilibrium point.

Some general control methods are:

- Proportional integral derivative(linear PID) control
- The sliding mode control scheme
- Dynamic evolution
- Model prediction control (Non-linear control technique)
- Boundary
- The fuzzy logic control method
- Digital control techniques

Switching strategies are:

- PWM (Pulse width modulation) control
- SPS (Single phase shift) control technique
- PWM-SPS (Phase shift + PWM)

PID controller has low cost, reliable, and excellent dynamic performance, but their efficiency and robustness for disturbances is very less. Sliding mode control has a speedy and finite response, robust for both large and small disorders, but its complexity is because of the specific parameters and state information requirement. Dynamic evolution has appropriate overall performance traits and not like SMC; it does no longer require precise knowledge of version parameters; however, it's miles hard to implement it in analog circuit shape. Model predictive management has reference monitoring and easy implementation, but it is restrained to the use of a linear converter model. Fuzzy logic control applies to the non-linear system also, and it is fast and robust. Digital control has high EMI immunity, flexibility, easy use, and low switching losses. Boundary control has a first massive signal operation, fast dynamics, but its cost is more and is sensitive to parameter variations.

B. Energy Storage systems

Electrical strength can be saved in lots of particular bureaucracy along with electrochemical energy, kinetic strength, ability power, and many others. This stored energy is then converted back to electrical form, but while conversion, some losses may be present. Energy storage systems can be considered as their essence for providing continuous, reliable, and sustainable electricity.

Batteries

Batteries are the electrochemical energy storage systems in which a pair of oxidation and reduction reaction (or redox reaction) occurs in an electrolytic medium to store DC power through the flow of ions and electrons. A battery cell comprises an external circuit and an internal circuit. The internal circuitry includes the electrodes, electrochemically active substances, and an electrolyte closed in a container. Fig shows the working of battery and movement of ions and electrons in both internal and external circuits.

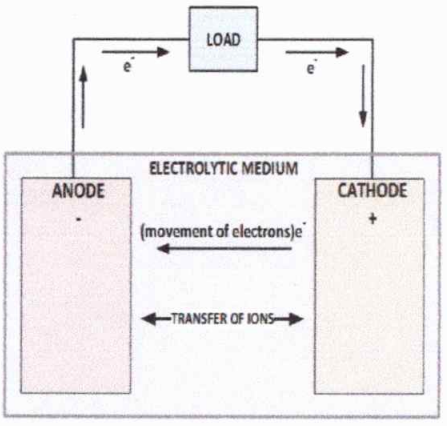


Figure **Error! No text of specified style in document.** Battery working model

Hybrid Energy Storage Systems (HESS)

Many energy storage are presently used, but no device can provide rapid response for a long time-span. Two essential terms are useful, especially while designing hybrid energy storage systems, namely Energy Density and Power density. The difference between these two is that a high energy density device can store the energy for a longer duration of time while power density describes the dynamics of the invention to deliver energy, i.e., its response. Energy density is defined in Watt-hrs/kg, whereas power density is defined in watts/kg.

II. PROPOSED CONFIGURATION

A. Proposed Topology

Figure 2 shows the schematic of the proposed topology. The given topology consists of a boost converter, a Bi-Directional DC-DC converter connected through inductors. The given topology has a boost converter with V_{DC} as input voltage, L as source inductance, a diode D, filter capacitance C_f, switch S, and a load resistance R_L. A bi-Directional buck-boost converter is chosen using a configuration similar to inverter two-leg configuration. Where the switches S1, S2 are connected in the first leg and switches S3, S4 are connected in the second leg. D1, D2, D3, D4 are the antiparallel diodes of switches S1, S2, S3, S4, respectively. To understand the working of the proposed topology, the modes of operation are explained in step by step manner as follows. First, the procedure is demonstrated using a single-leg structure, and then the control strategy for the two-leg system are explained.

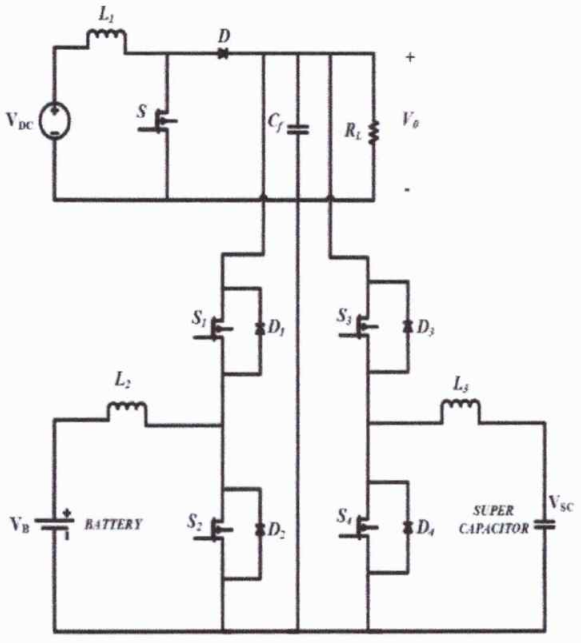


Figure **Error! No text of specified style in document.** Architecture of the microgrid system with battery and supercapacitor HESS.

B. DC Microgridconfiguration using the battery alone

A supply Bi-Directional DC-DC converter is used to modify the DC microgrid with the battery is attached proven in Fig.3 The Photovoltaic panel is designed for MPP voltage of 12V is emulated by way of using a regulated power supply of 0-24V/zero-3A and is hooked up the input to the raise converter.

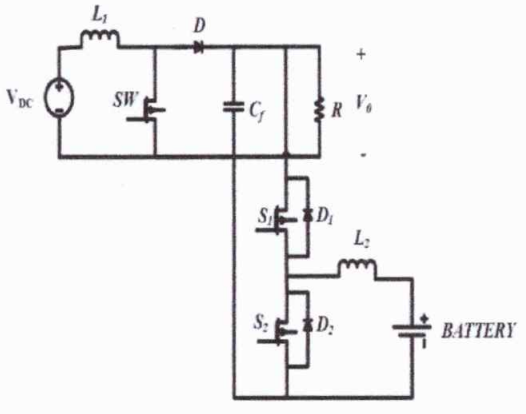


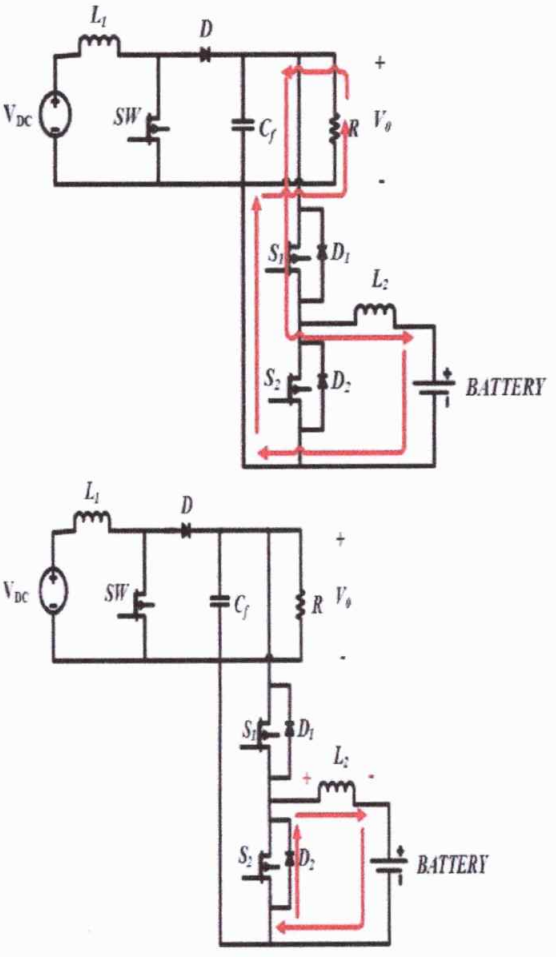
Figure 3. Architecture of the DC microgrid system with battery.

The output side of the boost converter, a battery, is connected using complementary switching devices.

In Fig 3 switches S1 and S2 are complimentary. Diodes D1 and D2 are the feedback diodes to switches S1 and S2, respectively. The high-frequency inductors L1 and L2 are connected to the boost converter and battery side. The high-frequency inductors are sufficiently high to make continuous conduction mode. (CCM) and to maintain constant DC. $C_f$is filter capacitance. It keeps output voltage ripple under control, and R is the load resistance.

C. Mode-I: Power flow from DC grid to the battery(charging mode)

The battery charging operation is explained in Fig.4. The battery charging is possible only when increasing PV generation or reducing the load demand. If PV generation increases load demand is constant, the excess power existing at the load side. According to the switching logic, excess energy charges the battery to maintain the grid voltage constant. In Fig 4(a) switches S1 turn ON and S2 turn OFF current flow from DC microgrid to the battery (charging operation of cell).



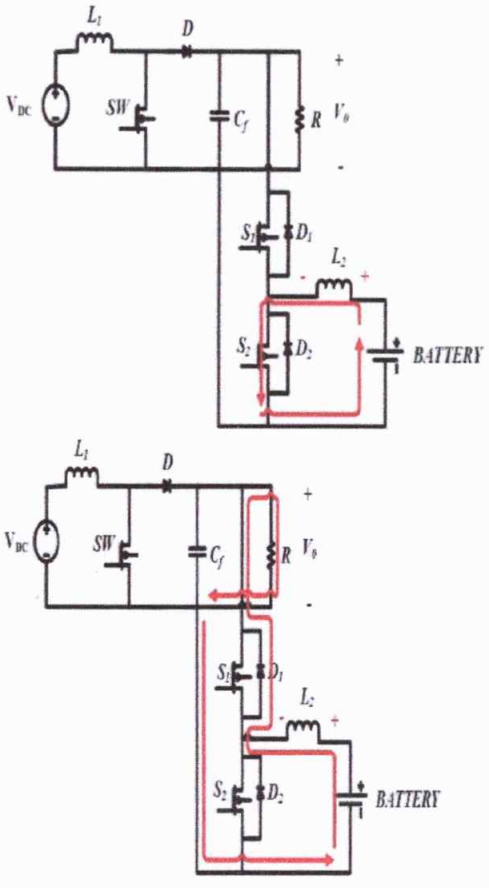
a) S1 ON, D2 OFF, S2 OFF, D1 OFF(b) S1 OFF, D2 ON, S2 OFF, D1 OFF

Figure 4 (a), (b)ESS charging operation (Buck Operation).

Later switch S_1 is turned OFF, and D_2 gets forward biased to store energy into the battery from the inductor, which is given in figure 4 (b). A solid line indicates the flow of current within the circuit.

d. Mode-II: ESS Discharging

The discharging operation of the battery is possible only when decreasing PV generation and increasing load demand. In this case, a deficit power exists at DC microgrid, immediately battery discharge to supply deficit amount of energy to maintain the grid voltage constant.



(a) S1 OFF, D2 OFF, S2 ON, D1 OFF (b) S1 ON, D2 OFF, S2 OFF, D1 OFF

Figure 5 (a), (b) ESS discharging operation (Boost Operation).

When DC grid voltage less than the PV generation, than immediately battery discharge and supply power to the DC grid to maintain the grid voltage constant. Switch S2 is turn ON and stores energy in an inductor by using a battery. Inductor stores energy as shown in with current directions, as shown in Fig 5(a). After the next switching state sum of battery voltage and inductor voltage is higher than DC grid voltage, than turn OFF the switch S2 and diode D1 turn ON, so power frow from the battery to DC grid to maintain the grid voltage constant. Bi-Directional power flow between source and load, as shown in Fig.6.

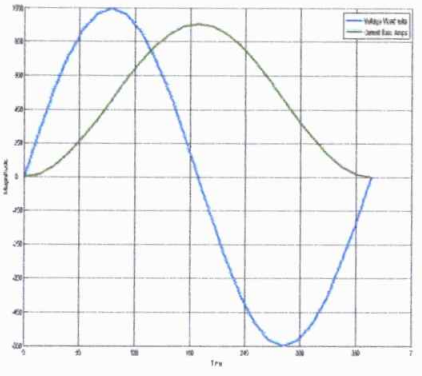


Figure 6 Graphical representation of bidirectional power flow.

III. CONTROL STRATEGY

A. Control Strategy for Battery Energy Storage System

A control scheme is implemented for stabilizing the DC grid voltage for source and load disturbance conditions. Switches are controlled according to the switching logic for charging/discharging operation of battery to maintain the DC grid voltage constant. Proportional integral controls scheme is used for controlling the switches in battery energy storage systems. For calculation of control gains, used single input single output (SISO) toolbox in MATLAB. For complete control, the tuning controller gains selected as 60 phase margin (PM).

Fig 7 represents the control scheme for battery alone DC microgridsystem. The total reference current, which is the input current of the boost converter, is compared with inductor current and error is applied to the PI controller. PI controller generated control signal depending upon error input. The pulse generator generates control pulses according tothe control signal. Under source and load power variations, DC grid may cause imbalance. To maintain the DC grid voltage constant charge/discharge battery to maintain the DC grid voltage constant.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

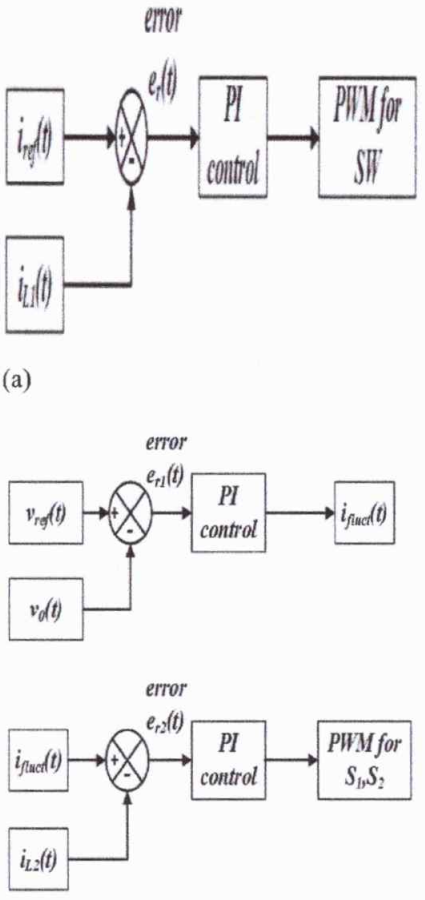


Figure 7 (a) Control logic of boost converter in BESS (b) Control logic of Bi-directional buck-boost converter for the battery.

A control scheme of the bidirectional converter is shown in Fig 7 (b). The reference voltage is compared with the actual DC grid voltage error is generated. The error is applied to the PI controller, and the controller generates a control signal. The pulse generator generates pulses according to the control signal. The controlled pulses are applied to the switches S1 and S2, which are complementary to each other.

IV. SIMULATION RESULTS

A. Simulation results for the proposed Scheme

Simulation results are developed using MATLABsoftware 2016 version. 12V, 7Ah Lead-acid battery used for this simulation. Switching frequency selected for this operation is 10 kHz. The input to the boost converter is taken as 10V with the help of DC Source. High-frequency inductor are designed for boost converter under ripple content. MOSFET switches are used for the simulation study of boost and bidirectional DC-DC converter.

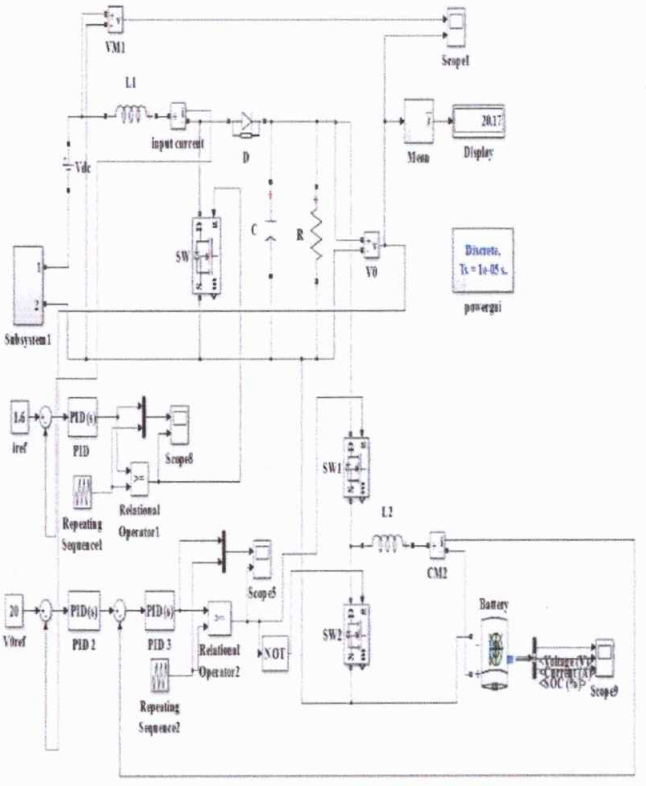


Figure 8 Simulation model for the battery alone system.

The simulation model for voltage regulation of DC microgridusing battery-based Bi-Directional DC-DC converter is illustrated in Fig.8

B. Simulation Results

In this segment, the results of the proposed technique are displayed, and two test cases are considered. The proposed Scheme has been made using dSPACE DS 1104 controller board. The control procedure is made using Simulink blocks in MATLAB. With the ultimate objective to exhibit the ampleness of the proposed procedure, it is differentiated and the traditional strategy. The model of lead-acid of 12V, 7Ah is utilized as a battery. Switching frequency is utilized for circuit operation is 10 kHz. With the assistance of a DC source, the PV output module is picked as 10V. In light of ripple content, the filter capacitance and inductor are intended for the boost converter. For boost and bi-directional DC-DC converters, MOSFET switches are chosen. The software

utilized and the hardware prototype created to execute the proposed Scheme likewise clarified in this segment. Experimental results are contrasted to simulation results. The proposed approach simulation results for two test cases are examined beneath.

Case.1: Battery Alone System

In this case, the single battery system is studied. The simulation diagram of voltage regulation of DC Microgridusing battery-based bi-directional DC-DC converter is depicted in Fig 8.

Step Increase in Source Voltage

Fig 9 (a) demonstrates the source voltage with disturbances over the period frame. Here, the source voltage is all of a sudden expanded at the time instant of t=1.5 sec which is kept up at 12V up to t=2 sec. At the point when there is no battery storage, and bi-directional converter, the output voltage of the boost converter is likewise expanded to a value of 24V amid this disturbance period. At the point when a bi-directional converter is associated with battery and grid, the grid voltage is recovered back to 20V utilizing the proposed control strategy

Step Decrease in Source Voltage

Fig 9 (b) demonstrates the source voltage with ESS over some time. The source voltage is all of a sudden diminished at the instant of time at t =0.5sec which is kept up at 8V up to t =1sec. At the point when there is no battery storage and bi-directional converter, then the boost converter output voltage is likewise diminished to a value of 16V amid this disturbance period. At the point when a bi-directional converter is associated with battery and the grid, the grid voltage is recovered back to 20V utilizing the proposed control strategy.

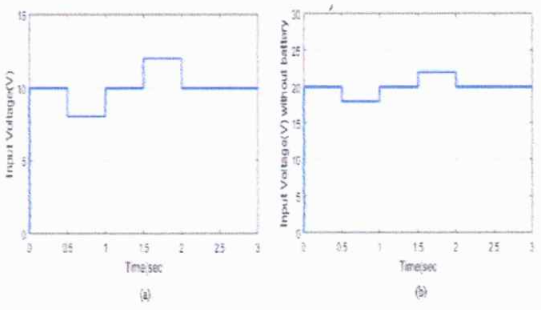


Figure 9 (a) Source Voltage With Disturbances (b) Load Voltage Without ESS

C. Performance Analysis of Battery Alone System

Fig 10. (a) demonstrates the graph of battery voltage versus time. It indicates battery performance amid step disturbance in the input voltage of the source converter. As it is observed from Fig 10 (a) the voltage in the battery is diminished to the operation of discharge from 0.5sec to 1sec amid step decrease in source voltage. Fig 10 (b) demonstrates the plot of battery current versus time. In input voltage of step decrease, current in the battery is controlled to supply the deficit voltage at the grid. Fig 4.4 (c) demonstrates the state of charge of a battery in (%). It is seen from the fig 10 (c) amid the duration of step decrease in source voltage, the battery current is expanded, and it keeps up a similar incentive till the disturbance is evacuated and SOC % of the battery diminishes. For step increase in input voltage, battery current is controlled to supply surplus voltage at the grid. For this, the battery voltage is expanded at t=1.5sec representing to the charging operation from 1.5sec to 2sec amid step increase in source voltage. It is seen from the fig 10 (c) battery current is diminished and keeps up the same value till disturbance is evacuated and SOC (%) of battery increments.

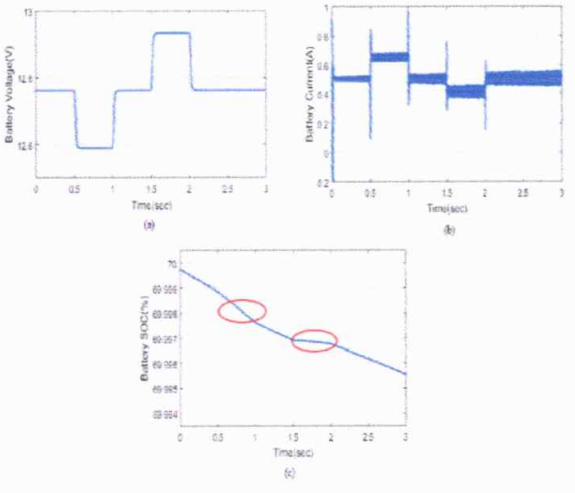


Figure 10 (a) Voltage (b) Current (c) SOC % of Battery

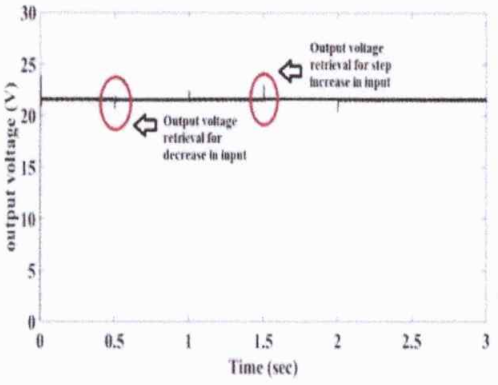


Figure 11 Output Voltage with Battery Energy Storage

The output voltage with BES demonstrates Fig 11. It outlines the recovery of output voltage while expanding or diminishing in the input voltage. As seen in Fig 11, amid the step decrease in source voltage, the output voltage is recovered at the time instant of t=0.5sec. After that the time instant of 1.5 sec, the output voltage is recovered amid the step increase in the source voltage.

V. CONCLUSION

A Bi-Directional converter is designed with a controller for the battery storage device. The performance of the ESS is analyzed for the supply version case. The controller ought to effectively stabilize DC microgrid against supply voltage variation. Charging and discharging waveforms of the battery are determined at some point in the supply voltage variant. The battery and superb capacitor blended energy garage is supplied. The electricity stability operation imposes extreme pressure on the battery if battery on my own is used as a strength garage medium. This is mainly because of the low strength density of battery. Thus, high strength density fantastic capacitor is mixed with excessive power density battery the usage of suitable manipulate approach to percentage the imbalance energy that exists between the supply and load of the microgrid.

REFERENCES

1. H-J. Kim, S-W. Kang, G-S. Seo, P Jang, and B-H. Cho, "Large signal stability analysis of DC power system with active shunt damper", IEEE Transactions on industrial electronics, vol. 63, no. 10, pp. 6270-6280, Oct. 2016.

2. Z. Zhao, J. Hu, and J. Liu, "Hierarchical coordinated control of multibus-based DC micro grid considering fault occurred buses," Proceedings of 2016 China International Conference on Electricity Distribution. Xian, Aug. 2016.

3. S. Sanchez and M. Molinas, "Large signal stability analysis at the common coupling point of a DC microgrid: a grid impedance estimation approach based on a recursive method" IEEETransactions on energy conversion, vol. 30, no. 1, pp. 122-130, Mar. 2015.

4. N. R. Tummuru, M.K.Mishra, and S. Srinivas, "Dynamic energy Management of renewable grid integrated hybrid energy storage systems," IEEE Transactions Ind. Electron., vol. 62,no. 12, pp. 7728–7737, Dec. 2015.

5. A technical guide in the year 2008 from NESSCAP ultracapacitor companyLimited.

INTERNATIONAL JOURNAL OF ENGINEERING INNOVATIONS IN ADVANCED TECHNOLOGY
ISSN [O]: 2582-1431 VOLUME-I ISSUE-II APR-JUN-2019

Compensation of Harmonics and Dynamic Reactive Power with Grid Interconnection using Shunt Hybrid Active Power Filter Control Technique

T.Kranthi kumar [1], Ragini[2]

[1]Asst.Prof. in Department of EEE,Avanthi institute of engineering & Technology(JNTUH), India.

[2] Asst.Prof. in Department of EEE,Avanthi institute of engineering & Technology(JNTUH), India

Abstract: *The matrix interconnection of sustainable power source is a mainstream issue in the electric utilities. Different sorts of converter topology in network interconnection have been enhanced by analysts to enhance control quality and effectiveness of the electrical system. The primary commitment of this paper is that shunt half and half dynamic power channel (SHAPF) with a DC-DC converter at dc connection is to give interconnection between sustainable source and network with direct unique burdens. The other commitment of this paper is to display a novel control system for responsive power pay and music disposal in modern systems utilizing a half and half dynamic power channel as a mix of a three stage, two level voltage source converter associated in parallel with single tuned LC aloof filter. In proposed control strategy, receptive power remuneration is accomplished effectively with discernible amount. Besides, the execution aftereffects of symphonious pay are acceptable. Hypothetical examinations and recreation results are gotten from a real mechanical system display in PSCAD. The reenactment results are introduced for proposed framework with a specific end goal to exhibit that the symphonious remuneration execution meets the IEEE-519 standard.*

***Keywords*—Harmonics, power quality, Reactive power compensation, grid, hybrid active power filters**

I. INTRODUCTION

By the advancement of technology, electric utilities and use of electric power are expanded. The greater part some portion of vitality request is given by petroleum derivatives. However, fossil fills are limited assets and will in the long run diminish. Due to this condition, they turn out to be excessively costly or too ecologically harming, making it impossible to recover. In the current years, renewable vitality in power era has been developing as an option vitality source to moderate the weaknesses of fossil fuels. In any case, the escalated utilization of nonlinear burdens cause a few power quality issues at PCC[1].The matrix voltages and streams shape non sinusoidal frame that is called symphonious twisting because of these sorts of burdens.

Consonant bends can build control misfortunes, as well as lessen the lifetime of types of gear. Keeping in mind the end goal to decrease the present symphonious contamination, detached channel is one of the customary arrangement ineffectively. These channels may bring about undesirable reverberation conditions. Their other restriction can't adjust to the changing conditions in the system and their size. With amazing procedure in the speed and limit of semiconductor exchanging devices, active channels have been contemplated and put into down to earth use, because they can beat the inconveniences inalienable in latent filters. These sorts of channels are more powerful in consonant pay and enhance execution [2]. However, dynamic power channels have high starting cost, running cost and required relatively high power converter ratings. To overcome the previously mentioned disadvantages, passive and dynamic channels can be consolidated into a solitary gadget called cross breed dynamic power channels (HAPF).HAPFs successfully smooth the issues of the detached channel and an dynamic power channel arrangement; consequently guarantee savvy consonant pay. The inactive channel in the framework performs essential sifting activity at the prevailing consonant frequencies, though the dynamic channel part mitigates higher music with exact control methods. This will successfully diminish the general size and cost of dynamic filtering. In expansion, no central voltage is connected to the dynamic part. This brings about an extraordinary decrease of the voltage rating of the dynamic power channel part.

A few half and half APF (HAPF) topologies [2- 11,15-17] constitute dynamic and detached parts in arrangement as well as parallel have been proposed for receptive power and consonant current separating in [3-15]

.The most normal topologies are shunt HAPF (SHAPF)[3-10] comprising of an APF and latent channel associated in arrangement with each other and arrangement HAPF[11] which is a joined arrangement of shunt aloof channel and arrangement APF. An broad diagram of the topological structures is clarified in [2].

The controller configuration is a critical and testing assignment because of its effect on the execution and soundness of general framework. Hence, various control techniques, for example, pq hypothesis [3-5], quick fourier change [5], dq hypothesis [6-7], fluffy controller [8-9], corresponding thunderous current controller [10] are controller techniques connected in writing.

Most learns about SHAPF in writing cannot accomplish dynamic receptive power pay [7-9]. Besides, SHAPF can remunerate the dynamic responsive power with steady dc interface voltage in [5]. In this article, coordinate current controlled heartbeat width adjustment is utilized. Furthermore, the dc connection is controlled as both dynamic and receptive current segment. The outcomes are acquired for low voltage level with remunerating little measure of receptive power. Besides, SHAPF can accomplish the dynamic responsive power pay with versatile dc connect voltage in [3]. Moreover, the dc connection is controlled as dynamic current part. The reference dc interface voltage might be lacking to track the new reference esteem when the versatile dc connect voltage might be changed from low level to abnormal state [5]. Moreover, when this dc connection is controlled as dynamic current segment, an additional start up precharging control circuit is required. In the last article [4], SHAPF can accomplish the dynamic receptive power pay with versatile dc interface voltage. Additionally, particular consonant pay is accomplished. The dc connection is controlled as both dynamic and receptive current segment as in [5]. The outcomes are gotten for 220 V, 10 kVA framework. Be that as it may, SHAPF repays little measure of receptive power.

The developing measure of electric vitality created from circulated or decentralized vitality assets (DER), for the most part of renewables, requires their suitable framework coordination. Accordingly, the sustainable power source interfacing with network is the real issue in the electric utility side. Distinctive sorts of converter topology in matrix interconnection have been enhanced by specialists to create control quality and proficiency of the electrical framework [12-13]. This paper centers the shunt cross breed dynamic channel interfaces for the sustainable power source with proposed controller.

Because of the constraints between existing writings, the reason for this paper is the accompanying:

1. To give interconnection between inexhaustible source and lattice by utilizing shunt half and half dynamic power channel (SHAPF) with unidirectional disengaged DC-DC converter at dc connection.
2. To present another control system for receptive power pay and music disposal.
3. To adaptively controlled dc connect voltage as receptive current segment.
4. To accomplish responsive power pay which is about equivalent to 99% of load receptive power limit.

As this paper fundamentally concentrates on the aforementioned four parts of the shunt crossover dynamic power channel.

II. PROPOSED SYSTEM AND CONTROLLER

Figure.1 exhibits the proposed SHAPF framework. As can be found in Figure 1 inverter unit is associated with the lattice through a LC channel tuned on the region of the fifth symphonious.

As can be found in Figure 2, the controller of proposed framework comprises of four principle parts: symphonious reference era, responsive current reference era, dc connect voltage controller, dc-dc converter controller and last reference pay current-pwm control square.

The consonant current control, receptive current control and dc connect control are accomplished by circuitous current control. With this control technique, any additional start up precharging control process is a bit much for dc interface. In addition, reactive power remuneration is accomplished effectively with distinguishable sum. Moreover, the symphonious pay execution is agreeable.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

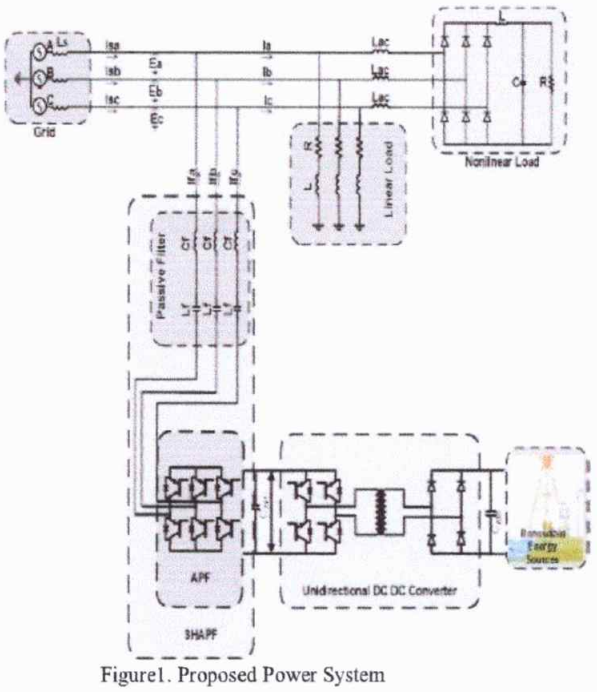


Figure1. Proposed Power System

A. Harmonic Current Control

The consonant control of SHAPF is appeared in Figure 2.The initial step is to seclude the symphonious parts from the central segment of the matrix streams. This is accomplished through dq change (1), synchronized with the PCC voltage vector, and a first request low pass channel with cut off recurrence of 10 Hz. At that point the dq reverse change (2) creates the symphonious reference streams in abc referential casing.

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta_p & \cos(\theta_p - 2\pi/3) & \cos(\theta_p + 2\pi/3) \\ -\sin\theta_p & -\sin(\theta_p - 2\pi/3) & -\sin(\theta_p + 2\pi/3) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_{a\_harmonic\_ref} \\ i_{b\_harmonic\_ref} \\ i_{c\_harmonic\_ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta_p & -\sin\theta_p & \frac{\sqrt{2}}{2} \\ \cos(\theta_p - 2\pi/3) & -\sin(\theta_p - 2\pi/3) & \frac{\sqrt{2}}{2} \\ \cos(\theta_p + 2\pi/3) & -\sin(\theta_p + 2\pi/3) & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_{d\_lpf} \\ i_{q\_lpf} \\ i_{o\_lpf} \end{bmatrix} \quad (2)$$

B. Reactive Power Control

Dynamic receptive power varieties in roughly 20% happened in load are repaid by inverter side of SHAPF. The reference current gave fundamental responsive power is delivered. Keeping in mind the end goal to accomplish the responsive power remuneration of SHAPF, the reference current having 90° stage contrast among the PCC point ought to be delivered. To create this reference current, the yield voltage of SHAPF inverter ought to be produced in stage with PCC voltage vector. The square graph of receptive power control is appeared in Figure 2.

The reference streams ought to be ascertained to remunerate receptive power in the framework. The reference streams are produced by the dq strategy. The initial step is to seclude the crucial parts from the consonant segments of the matrix streams. This is accomplished through the dq change (3). The quadrature part of the source current which is taken from dq change is straightforwardly gone through the LPF. Subsequently, the 50 Hz part of the source current is produced. At that point, this flag is connected to deliver the responsive power pay current by inversing dq change. Nonetheless, this reference current is in quadrature hub. To accomplish receptive power pay by voltage controlled voltage source SHAPF, the reference current must be in stage with source voltage. In this way, the reference current is changed by utilizing just d part reverse dq change (4).

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta_p & \cos(\theta_p - 2\pi/3) & \cos(\theta_p + 2\pi/3) \\ -\sin\theta_p & -\sin(\theta_p - 2\pi/3) & -\sin(\theta_p + 2\pi/3) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} i_{a\_reactive\_ref} \\ i_{b\_reactive\_ref} \\ i_{c\_reactive\_ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta_p & -\sin\theta_p & \frac{\sqrt{2}}{2} \\ \cos(\theta_p - 2\pi/3) & -\sin(\theta_p - 2\pi/3) & \frac{\sqrt{2}}{2} \\ \cos(\theta_p + 2\pi/3) & -\sin(\theta_p + 2\pi/3) & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_{d\_lpf} \\ 0 \\ 0 \end{bmatrix} \quad (4)$$

C. DC Link Voltage Controller

Figure.2 demonstrates the square graph of the dc connect voltage controller. The initial step is to figure the quick load receptive power.

At that point utilizing the d and q part both three stage network voltage and current, the prompt load receptive power is computed. In next process, the reference dc connect voltage is resolved with the condition [3] appeared in Figure 2.

Figure 2 shows the control of the blunder flag. The blunder flag is controlled by regular PI controller [6].

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

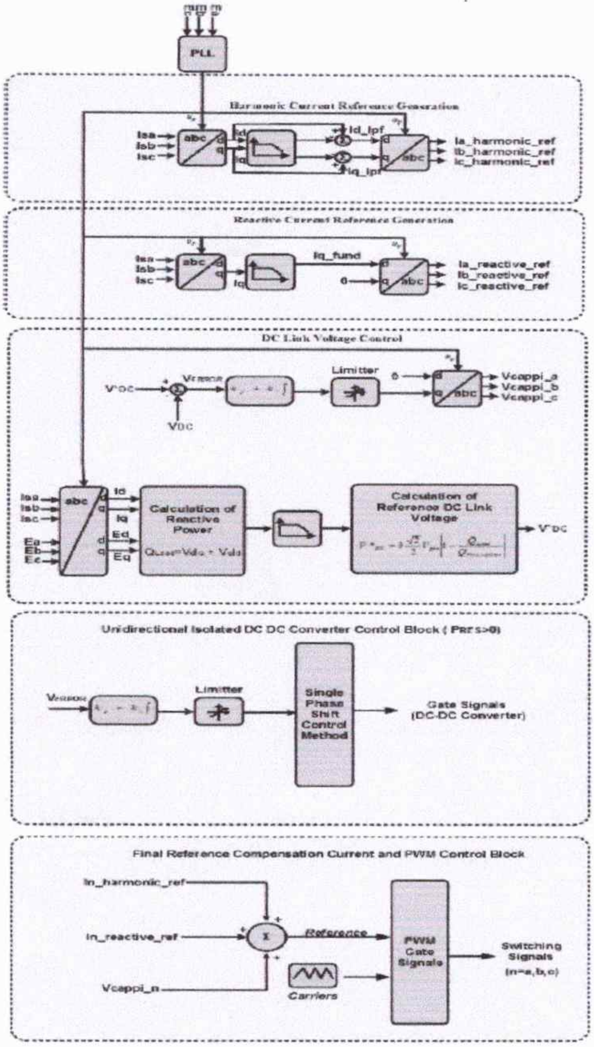


Figure.2. Proposed Controller Block Diagram

D. DC-DC Converter Controller

Single stage move (SPS) control technique which is the most generally utilized is connected for the proposed framework. In SPS control, the cross-associated switch matches in both full extensions are changed thus to produce stage moved square waves with half obligation proportion to the transformer's essential and optional sides. Just a stage move proportion (or point) D can be controlled. Through modifying the stage move proportion the equal air conditioning yield voltages of full-scaffolds, the voltage over the transformer's spillage inductor will change. Then, the control stream course and extent can be effectively controlled. A broad review of this control strategy is clarified in [14].

For the proposed framework, the power stream is acknowledged from RES to SHAPF. Hence, dc-dc converter create negative stage move plot for this power stream heading. This stage move point is controlled by basic PI controller.

This converter just performs when PRES>0 where PRES is the power created from RES appeared in Figure3.

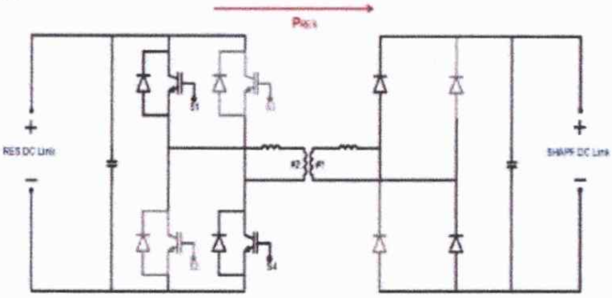


Figure.3. Unidirectional Isolated DC-DC Converter and Power Flow Direction

E. Final Reference Compensation Current and PWM Control Block

The last reference current comprises of three stage consonant reference current signs, three stage receptive reference current signs and dc interface control signals. The reference flag (In_harmonic_ref + In_reactive_ref +Vcappi_n) is created utilizing these signs together. Then,the reference signs are contrasted with bearer motion with produce exchanging signals appeared in Figure 2.

III. SIMULATION RESULTS

Reenactment studies are completed utilizing PSCAD/EMTDC. The principle reason for the reproduction is to assess the viability and accuracy of the control system utilized as a part of the SHAPF with varieties of straight loads.Parameters utilized as a part of reenactments are given in Table I. In reproduction, the ostensible recurrence of the power framework is 50Hz and the symphonious current source is produced by the three stage diode rectifier. Likewise, the dynamic receptive power changing is produced by direct loads appeared in Table II. The stage to stage lattice voltage is chosen as 380 V (crest peak).Passive channels are tuned at fifth and the control signs of IGBTs are created through the beat width adjustment generator whose adequacy and recurrence of transporter wave are ± 1 and 20 kHz, separately. The latent channel part bolsters a settled receptive power which is equivalent to 10 kVAR. The receptive power limit of the nonlinear load is 2 kVAR.

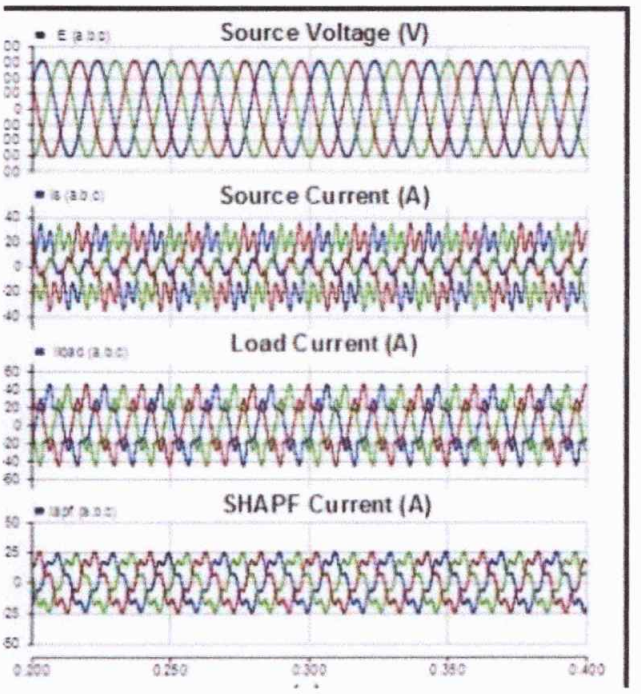
In this area, two method of operation are talked about in reenactment cases. A sustainable power source (RES) is associated on the dc connection of framework interface SHAPF. The primary point of proposed approach is to manage the power at PCC during: 1) PRES>0 and 2) PRES=0 where PRES is the power created from RES. While playing out the power administration operation, the SHAPF is effectively controlled in such a path, to the point that it generally draws/supplies major dynamic power from/to the matrix. At first, the SHAPF is not

associated with the system. Before time t=0.5s, the source, load and SHAPF streams are shown in Figure 4 (a).

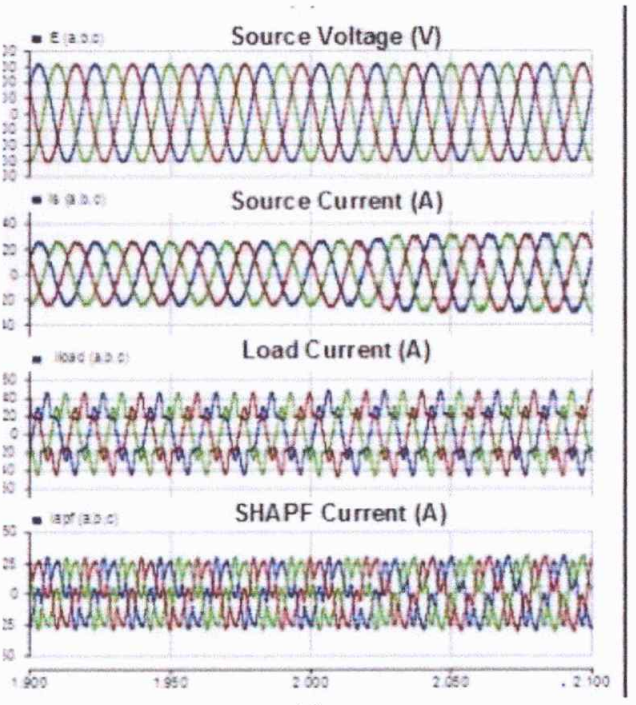
Initially method of operation considers a situation where PRES>0, the SHAPF infuses RES dynamic power into lattice and furthermore upgraded the nature of energy at PCC. Before time t=1s, RES is not associated with the system. The source, SHAPF and load dynamic power are appeared in Figure 5(a). At t=1 s, the RES associated with the system. The SHAPF begins infusing dynamic power created from RES as appeared in Figure 5 (b). Furthermore, SHAPF remunerates sounds effectively as appeared in Figure 4 (b).

Second method of operation considers a situation when there is no power era from RES. The SHAPF is to upgrade the nature of energy at PCC. The proposed control technique for dynamic responsive power pay with flexible dc connect voltage will be checked by reproductions. At the point when the stacking responsive power utilization is more prominent than given by the uninvolved channel part, the inverter side of the SHAPF can repay the rest of energy of the inactive channel. At time t= 2 s, the fourth load is associated with the framework. The receptive power rating of burdens is expanded 12kVAR. At the point when the heaps are associated with the framework, the framework gives a dynamic reaction. In this manner, the inverter side is remunerated the responsive power remainded by aloof channel limit. The source receptive power is about equivalent to zero appeared in Figure 5 (c). The lessened THD of the source current, while remunerating these heaps varieties, working adjusted supply implies in every one of the cases, sinusoidal current is drawn from the source appeared in Figure 4 (c). SHAPF dc connect voltage is adaptively changed from 160 to 225V appeared in Figure 5 (c). The measure of source side receptive power remains almost zero. In 2.5 s, the fifth load is associated with the framework. The receptive power rating of burdens is expanded 13kVAR. The inverter side is remunerated remainded by aloof channel limit. The measure of source side responsive power likewise remains almost zero appeared in Figure 5 (d).

The dc connect voltage of SHAPF is adaptively changed from 225 to 290V appeared in Figure 5(d). The lessened THD of the source current, while repaying these heaps varieties, working adjusted supply implies in all the cases, sinusoidal current is drawn from the source appeared in Figure 4(d).

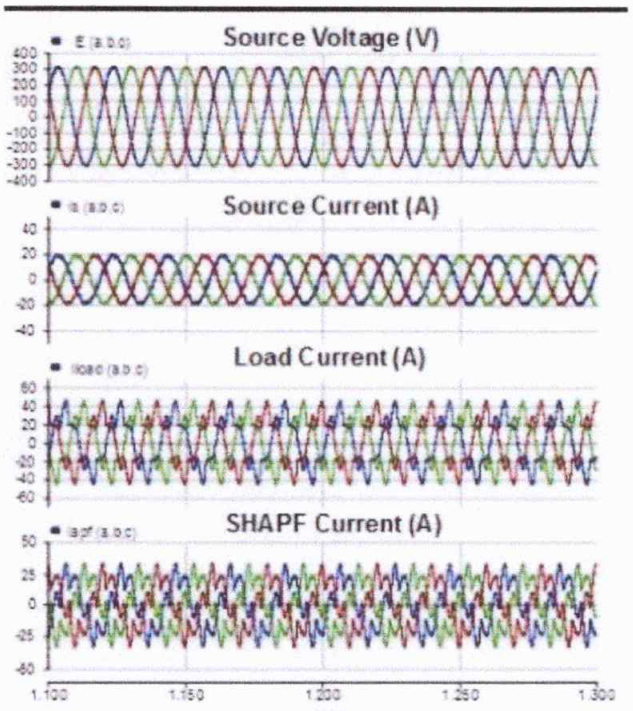


(a)

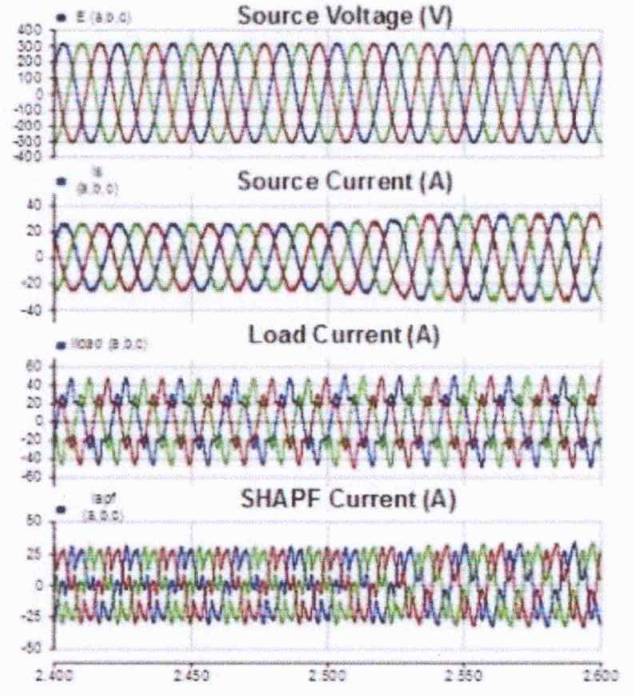


(c)

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist



(b)



(d)

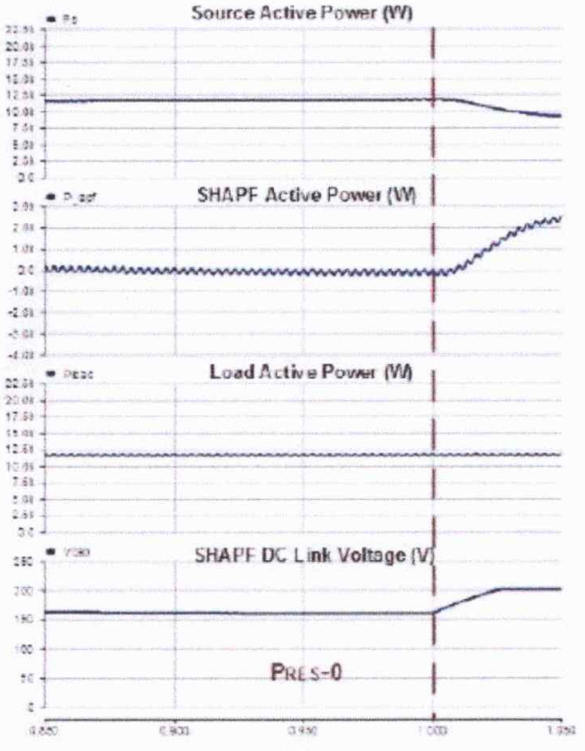
Figure.4. Three phase Source Voltages, Source - SHAPF - Load Currents (a)when SHAPF is not operated, (b) when PRES>0, (c) when PRES=0 and 1kVAR loads are connected (d) when PRES=0 and another 1kVAR loads are connected

Compared the simulation results with dynamic load changes, the proposed method can:

1) Interconnect between renewable source by using shunt hybrid active power filter (SHAPF)
2) Provide dynamic reactive power compensation
3) Reduce the THD of source side current
4) Adaptively change the dc link voltage value

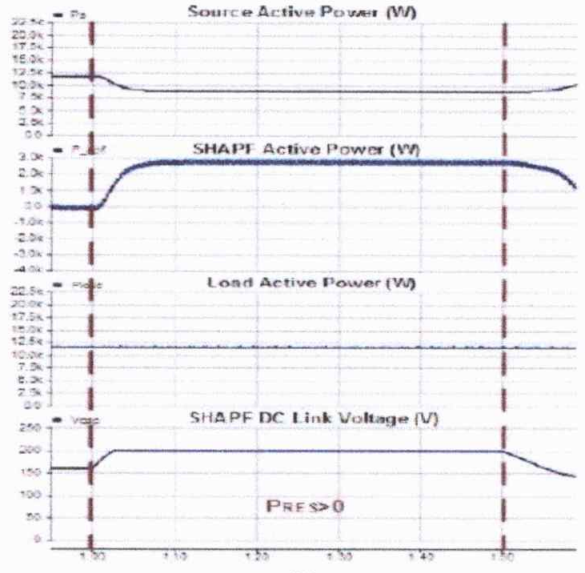
TABLE I. SIMULATION PARAMETERS

Parameters	Value
Line frequency	380 V
Filter Capacitor (CF)	50 Hz
Filter Inductance (LF)	200 µF
Tuned freq. of series filter(ftuned)	2 mH
Filter Capacitor (CF)	250 Hz
Load Inductances(Lac1	) 2.7 mH
Switching frequency (fswitching)	20 kHz
Simulation Step Time	40 µs
DC Link Reference Value	100-300 V
DC link Capacitors	12 mF

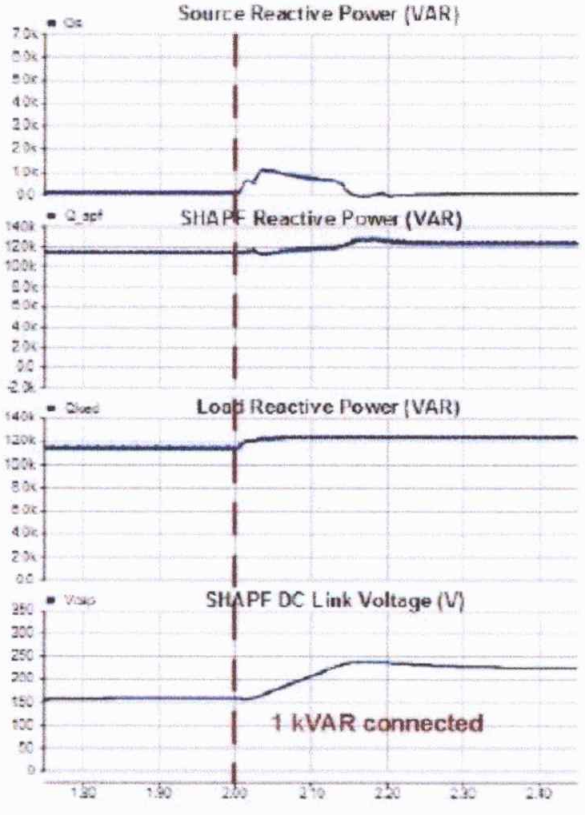


(a)

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist



(b)



(c)

Figure.5. Source - SHAPF - Load Active power and SHAPF DC link voltage when PRES=0, (b) Source - SHAPF - Load Active power and SHAPF Dc link voltage when PRES>0, (c) Source - SHAPF - Load Reactive power and SHAPF DC link voltage when PRES=0 and 1kVAR loads are connected.

TABLE I.SIMULATION PARAMETERS FOR TESTING LOADING

Inductive Loads	Physical Value	Reactive Power Capacity
1st Load (Rload1 Lload1)	5 - 90 mH	5kVAR
2nd Load (Rload2 Lload2)	10 - 225 mH	2kVAR
3rd Load (Rload3 Lload3)	10 - 225 mH	2kVAR
4th Load (Rload4 Lload4)	20 - 450 mH	1kVAR
5th Load (Rload5 Lload5)	20 - 450 mH	1kVAR

As a result, it is clearly shown that shunt hybrid active power filter (SHAPF) with a DC-DC converter at dc link achieves interconnection between renewable source and grid with linear dynamic loads. Besides, SHAPF using the proposed method can provide better compensation performance both harmonic and dynamic reactive power compensation.

IV. CONCLUSION

In this paper, SHAPF gives interconnection between sustainable source and matrix with direct unique loads. Besides,the novel control plot for SHAPF is proposed in order to remunerate both consonant and dynamic responsive power with versatile dc connect voltage. The fundamental commitments of this paper are:

- The matrix interconnection is provided by SHAPF for the sustainable power source.
- To present another control procedure for receptive power remuneration and sounds disposal.
- To adaptively controlled dc interface voltage.
- To accomplish receptive power remuneration which is almost equivalent to 100% of load responsive power limit.

The symphonious current control, the dc interface control and receptive current control are accomplished by backhanded current control. With this control technique, any additional start up precharging control process is a bit much for dc connect. Also, responsive power remuneration is accomplished effectively with detectable sum. Additionally, the symphonious remuneration execution is palatable.

In a conclusion, the SHAPF infuses RES dynamic power into lattice and furthermore improved the nature of energy at PCC. Reenactment consequences of the three-stage three-wire SHAPF in unique responsive power remuneration.

REFERENCES

[1] L. Herman, I. Papic, and B. Blazic, "A Proportional-Resonant Current Controller for Selective Harmonic Compensation in a Hybrid Active Power Filter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5,pp. 2055– 2065, Oct. 2014.

[2] A. Chowdhury, C. Rajagopalan, and M. A. Mulla, "Compensation of three-phase diode rectifier with capacitive filter working under unbalanced supply conditions using series hybrid active power filter,"
IET Power Electronics, vol. 7, no. 6, pp. 1566–1577, Jun. 2014.

[3] P. Neves, D. Goncalves, J.G. Pinto, R. Alves, R.,"Single-phase shunt active filter interfacing renewable energy sources with the power grid," In: Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE; 3-5 November 2009; Porto, Portugal: IEEE. pp. 3264 – 3269.

[4] K. Ilango, A. Bhargav, A. Trivikram, P. S. Kavya, G. Mounika, and M. G. Nair, "Performance comparison of shunt active filter interfacing algorithm for renewable energy sources," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE*
International Conference on, 2012, pp. 1–6.

[5] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual -Active- Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[6] S. Rahmani, A. Hamadi, K. Al-Haddad, and L. A. Dessaint, "A Combination of Shunt Hybrid Power Filter and Thyristor-Controlled Reactor for Power Quality," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2152–2164, May 2014.

[7] M. Salehifar and A. Shoulaie, "Hybrid active filter for harmonic suppression and reactive power compensation," in *Technical Postgraduates (TECHPOS), 2009 International Conference for*,2009, pp. 1–4.

[8] Z.Wei, L. An, P. Jianchun, D. Xia, and others, "A new hybrid active power filter for harmonic suppression and reactive power compensation," in *Electricity Distribution, 2008. CICED 2008. China International Conference on*, 2008, pp. 1–7.

[9] J. Wu, A. Luo, S. Peng, F. Ma, Z. Zeng, and M. T. Chau, "System control of hybrid active power filter for reactive power compensation and harmonic suppression," in *Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on*, 2011, pp. 862–866.

[10] L. Herman, I. Papic, and B. Blazic, "A Proportional-Resonant Current Controller for Selective Harmonic Compensation in a Hybrid Active Power Filter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5,pp. 2055– 2065, Oct. 2014.

[11] M. Singh, V. Khadkikar, A. Chandra, and R. K. Varma, "Grid Interconnection of Renewable Energy Sources at the Distribution Level With Power-Quality Improvement Features," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 307–315, Jan.
2011.

[12] Y. Deng , H. Jia and X. Tong, "A Bidirectional Control Principle of Active Tuned Hybrid Power Filter Based on the Active Reactor Using Active Techniques," IEEE Transactions on Industrial Informatics,vol. 11, no. 1, pp. 141–154, Feb. 2015.

[13] T.-L. Lee, Y.-C. Wang, J.-C. Li, "Hybrid Active Filter With Variable Conductance for Harmonic Resonance Suppression in Industrial Power Systems," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 746–756, Feb. 2015.

[14] L. R. Limongi, L. R. da Silva Filho, L. G. B. Genu, F. Bradaschia, "Transformerless Hybrid Power Filter Based on a Six-Switch Two-Leg Inverter for Improved Harmonic Compensation Performance," IEEE Transactions on Industrial Electronics, vol. 62, no. 1, pp. 40–51, Jan. 2015.

[15] J. Turunen, M. Salo, and H. Tuusa, "Comparison of three series hybrid active power filter topologies," in *Harmonics and Quality of Power, 2004. 11th International Conference on*, 2004, pp. 324–329.

[16] C.-S. Lam, W.-H. Choi, M.-C. Wong, and Y.-D. Han, "Adaptive DCLink Voltage-Controlled Hybrid Active Power Filters for Reactive Power Compensation," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1758–1772, Apr. 2012.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Md!) R.R.Dist

ગુજરાત સંશોધન મંડળનું ત્રૈમાસિક

JOURNAL
OF THE
Gujarat Research Society
"DO RESEARCH FOR GOOD OF MANKIND" Jawaharlal Nehru.
14-1-57

Journal of The Gujarat Research Society

Aqaaaaaa Study Of Ultrasonic Metal Welding To Achieve Quality Welds

Ramesh Babu Yeluri, Dr. P Manoj Kumar

Abstract

ગુજરાત સંશોધન મંડળનું ત્રૈમાસિક

JOURNAL OF THE Gujarat Research Society
"DO RESEARCH FOR GOOD OF MANKIND "—Jawaharlal Nehru.

Journal of The Gujarat Research Society

Aqaaaaaa Study Of Ultrasonic Metal Welding To Achieve Quality Welds

Ramesh Babu Yeluri, Dr. P Manoj Kumar

Abstract

Several Difficulties Are Faced In Joining Thinner Sheets Of Similar And Dissimilar Materials From Fusion Welding Processes Such As Resistance Welding And Laser Welding. Ultrasonic Metal Welding Overcomes Many Of These Difficulties By Using High Frequency Vibration And Applied Pressure To Create A Solid-State Weld. Ultrasonic Metal Welding Is An Effective Technique In Joining Small Components, Such As In Wire Bonding, But Is Also Capable Of Joining Thicker Sheet, Depending On The Control Of Welding Conditions. This Study Presents The Design, Characterisation And Test Of A Lateral-Drive Ultrasonic Metal Welding Device. The Ultrasonic Welding Horn Is Modelled Using Finite Element Analysis And Its Vibration Behaviour Is Characterised Experimentally To Ensure Ultrasonic Energy Is Delivered To The Weld Coupon. The Welding Stack And Fixtures Are Then Designed And Mounted On A Test Machine To Allow A Series Of Experiments To Be Conducted For Various Welding And Ultrasonic Parameters. Weld Strength Is Subsequently Analysed Using Tensile-Shear Tests. Control Of The Vibration Amplitude Profile Through The Weld Cycle Is Used To Enhance Weld Strength And Quality, Providing An Opportunity To Reduce Part Marking. Optical Microscopic Examination And Scanning Electron Microscopy (SEM) Were Employed To Investigate The Weld Quality. The Results Show How The Weld Quality Is Particularly Sensitive To The Combination Of Clamping Force And Vibration Amplitude Of The Welding Tip.

Published

Several Difficulties Are Faced In Joining Thinner Sheets Of Similar And Dissimilar Materials From Fusion Welding Processes Such As Resistance Welding And Laser Welding. Ultrasonic Metal Welding Overcomes Many Of These Difficulties By Using High Frequency Vibration And Applied Pressure To Create A Solid-State Weld. Ultrasonic Metal Welding Is An Effective Technique In Joining Small Components, Such As In Wire Bonding, But Is Also Capable Of Joining Thicker Sheet, Depending On The Control Of Welding Conditions. This Study Presents The Design, Characterisation And Test Of A Lateral-Drive Ultrasonic Metal Welding Device. The Ultrasonic Welding Horn Is Modelled Using Finite Element Analysis And Its Vibration Behaviour Is Characterised Experimentally To Ensure Ultrasonic Energy Is Delivered To The Weld Coupon. The Welding Stack And Fixtures Are Then Designed And Mounted On A Test Machine To Allow A Series Of Experiments To Be Conducted For Various Welding And Ultrasonic Parameters. Weld Strength Is Subsequently Analysed Using Tensile-Shear Tests. Control Of The Vibration Amplitude Profile Through The Weld Cycle Is Used To Enhance Weld Strength And Quality, Providing An Opportunity To Reduce Part Marking. Optical Microscopic Examination And Scanning Electron Microscopy (SEM) Were Employed To Investigate The Weld Quality. The Results Show How The Weld Quality Is Particularly Sensitive To The Combination Of Clamping Force And Vibration Amplitude Of The Welding Tip.

Published
2019-12-30

Issue
Vol. 21 No. 17 (2019): Vol 21 No. 17 (2019)

Section
Articles

International Journal of Management (IJM)
Volume 11, Issue 3, March 2020, pp. 831–836, Article ID: IJM_11_03_087
Available online at https://iaeme.com/Home/issue/IJM?Volume=11&Issue=3
ISSN Print: 0976-6502 and ISSN Online: 0976-6510
DOI: https://doi.org/10.17605/OSF.IO/2ZUXJ

COMPETENCY ANALYSIS

Dr. Y Jayaprada

Dr. Sushil Beliya

ABSTRACT

In today's competitive and global environment it has become crucial for every organization to retain competent employee for survival. The success of an organization depends not only on how the organization makes the most of human competences, but also how it stimulates commitment to an organization. Employee commitment, together with a competent workforce, seems to be of decisive importance for an organization to be able to compete in quality and to go along with changes. This paper reviews the available literature on competency based management and its uses in the organizational sector. Very little research has been done in this area in the Indian organizations. This paper defines the concept of competency based management, the driving force behind the use of competency based management and its uses in the organization as well as the future prospect of research in this area specifically in the Indian organization context. Organizations are using competency based management as a tool for the success of the organization. Studies have shown that competency approach to human resource management is not new. Competency framework is used by the organizations today in different HR practices like recruitment and selection, training and development, performance management, career development, compensation and pay etc. to improve the performance of the organization as well as of employees. Competency based management approach focuses on increasing the potential of employee to have the competitive edge over other organizations in today's time. Researchers and scholars have reported that competency based management has a positive effect on the performance of organization and on employee's performance also. Keyword: competency based management, organizational performance.

Keywords: Competency Analysis, HR Practices, Environmen, Organizational

Cite this Article: Dr. Y Jayaprada and Dr. Sushil Beliya, Competency Analysis, International Journal of Management (IJM), 11 (3), 2020, pp. 831–836.
https://iaeme.com/Home/issue/IJM?Volume=11&Issue=3

INTRODUCTION

In the present business environment of cut throat competition and globalization, competency based practices have gained much of an attention from the contemporary organizations. Globalization, individualization, digitalization and increasing competition are changing the face of the industry as we know it. They aim at achieving an optimum performance in the long term by developing the skills and competencies of the employees on a continuous basis. Literature and best practices indicate that, to some extent, if employers treat their employees as valued contributors, they tend to remain in the organization. To this end, organizations train, offer competitive compensation plans and increase benefits to secure their employee loyalty.

What Would Competency Analysis Mean?

Competency analysis is used to develop competency profiles and frameworks for HR planning, recruitment, performance management, and training and development. However, it can also give information for competence-related page processes, and the findings of the analysis can be used to define roles or contribute to the design of layers in a work family.

It is required to determine the knowledge, skills, and process abilities needed to accomplish the organization's business activities so that they may be established and used as the foundation for workforce practices

Competency Analysis Characteristics

Competencies have important characteristics:

They provide a clear framework and emphasis for recruitment, evaluation, performance review, and training, and they serve as the foundation for consistent staff selection and growth.

They defined the essential abilities that lead to effective job performance at the individual level.

They give the organization a common language by providing a systematic manner of describing activity.

They are primarily concerned with future behavior.

Competency Analysis' Objectives

Competency analysis is formalized to guarantee that it is carried out in accordance with established organizational processes.

The workforce competencies required to carry out the business activities of the organization are defined and updated.

The company keeps track of how well it does in each of its employee capabilities.
Work processes are established and managed for each worker capability.

METHODOLOGIES AND TOOLS FOR IDENTIFYING COMPETENCIES

(a) Workshops: A workshop with a more structured approach is more likely to deliver better results, especially if the workshop is primarily made up of people who are really doing the job. The skill definitions will thus be stated in the lingua of the jobholders, making them far more satisfactory and practical.

The workshop launch pad's responsibilities include assisting the group in analyzing its findings, prompting, providing examples, and generally assisting in the prediction of a set of competence dimensions that can be demonstrated through behavior-based examples.

The launch pad may have some ideas about the types of headings that might emerge from this process, but he or she should not try to persuade the group to reach a conclusion that it hasn't come to on its own, albeit with some direction.

(b) Expert Advice: The easiest technique is for a panel of 'experts' (members of the people department and line management representatives) to get together and create a data list based on their own sense of 'what counts,' potentially with the help of other published lists. It will save time and effort, but it may not be particularly analytical, and relying on other people's ideas may result in a list that is irrelevant to the business's true goals and requirements. While developing generic or particular role competencies, it's critical to make sure they flow directly from the company's core competencies, so people skills are properly integrated with and support business skills.

(c) Observation Method: While engaging with individuals, leading coworkers, learning new elements, and executing them, resource individuals notice top and average performers while working and taking divisions. The first part of such a report usually contains the observer's own interpretation and analysis of the observations, while the second half contains the observer's own interpretation and analysis of the observations. This observation of extreme performers in action help in establishing the competencies needed to do a task or work in the most effective manner, as well as what inadequacies or incompetence lead to average performance. The effectiveness of this method, however, is dependent on the observers' objectivity and neutrality.

(e) Questionnaire Method: The questionnaire approach is the most popular and extensively utilized tool for measuring competencies. This method can be used to assess competency at all three levels: organization, function, and job.

(d) Story Writing Method: Using this strategy, employees and their superiors will be asked to define the jobs they perform, as well as the knowledge, talents, and behavioral attributes necessary to complete them with quality, precision, and outcomes. Writings from all employees and supervisors are gathered and reviewed at the organizational level to determine competency requirements for various positions and responsibilities.

(e) Interview Technique: Interviewing current employees to determine what skills are required to execute a job. Job effectively gives useful information that aids in the identification of a job's most appropriate capabilities. To collect information, resource workers who have been educated in the interview approach use both a standardized and a contingency format.

There is a combination of structured and open-ended questions in the format. Depending on the scope of the study, these interviews will be conducted on all or a representative sample of employees. In the same way, interviewing the head of department or the chief executive may reveal function and organizational level competencies.

(f) Repertory Grid: In some aspects, this technique is similar to the critical incident strategy. The dimensions of excellent and poor performance standards are established using a repeatable grid. These traits were developed through interviews and surveys with job seekers to see what behaviors cause some people to perform extraordinarily well while others do not.

(g) 360- Degree Survey: Collecting feedback and viewpoints from our stakeholders on what competencies are wanted and required to effectively lead an organization, manage departments, and perform various duties generates a lot of data. Questionnaires, essay writing, debates, and conferences can all be used to gather data from a variety of stakeholders with varying degrees of expertise.

(h) Critical Incident Methods: Major incidents can reveal a lot about the skills needed to deal with them, whether they resulted in remarkable outcomes or failures for organizations and individuals. Using this strategy, a few examples from the past or scenarios that are likely to occur in the present or future will be chosen for a given research.

Both observers and job holders will write a descriptive version of the incident's origin, how it was handled, why one strategy was chosen over another, what knowledge, expertise, or soft skills were employed in resolving the incident, and what outcomes were predicted and actually achieved. This method's data is very useful for identifying significant competitors.

(i) Focus Groups: Employees that perform extraordinarily well, are innovative, and have a history of questioning the status quo comprise a focal group in this strategy. To achieve great results, this group focuses on identifying and suggesting the optimum competency model to deploy at the organizational, functional, and job levels.

(j) Case Study Method: Highly successful performances that employees enjoy and perceive as the best of their careers in an organization, as well as underperformance events, are researched in depth to understand the factors that contribute to peak performance and the variables that contribute to below average performance. It is determined which abilities are required to properly manage adverse conditions and which abilities are required to establish conducive situations for superior performance. When a thorough investigation is necessary, the case study method is applied. The study is carried out by resource persons using organized and unstructured information gathering approaches.

Advantages of Competency Analysis

Competency analysis serves as the cornerstone for a number of human resource development efforts. This versatile, flexible, and scalable tool has been used to accomplish the following:

Concentrate on improving your performance.

Encourage employees to improve their performance on a regular basis.

Determine whether or not an individual is ready for a promotion.

Employees' career development should be guided.

Concentrate your training on the skills that need to be improved.

Give credit where credit is due for prior knowledge and expertise.

Assist in the development of human resources in a systematic manner.

Individualize training delivery to meet the needs of the individual or business.

Examine if training programmes are appropriate for promoting job competence.

Employees should be given a precise work description.

Create job postings,

Personnel should be interviewed and chosen.

Perform performance evaluations,

Create a modular training programme that can be grouped as needed.

Create a learning programmer

CONCLUSION

It is visible from the literature review that competency based management is a fast emerging as a new approach for making employees more proficient in their work so that organizations can achieve the competitive edge over their competitors and thrive in today's time. Competency based management have turned out to be an effective tool for HR to improve the organizational performance. Integration of competency model with the HR function has enhanced the performance of individual as well as organization.

FUTURE DIRECTIONS

Competency approach has been in practice from past 30 years for managing the human capital of any organization, it shows that it's not something new. However, this concept has not been explored much in the Indian Context. As the business Competency Based Management In Organizational Context: A Literature Review 355 environment is changing frequently due to various developments in the technical, social and economic environment the role of organizations using competency framework for human resource management should be studied for retaining the employees and to increase the commitment of the employee towards the organization as having a competent pool of employees have turned out to be a crucial part of any organizations. Effect of implementing competency based management in the different organizations need to be further explored as it will help in improving and gaining insight of the concept which in turn will help the organization in enhancing their performance as well as that of employee.

REFERENCES

[1] Ashkezari M J D, Aeen M N. Using Competency Models to Improve HRM. Ideal Type of Management 2012; 1(1): 59-68

[2] Boyatzis, R.E. (The Competent Manager: A Model for Effective Performance. Wiley, 1982; New York, NY.

[3] Byham. Developing Dimension/Competency-Based Human Resource Systems: A Monograph, 2006.

[4] Caupin. ICB – IPMA Competence Baseline, version 3.0. International Project Management Association 2006.

[5] Cook, Kevin, Bernthal, Paul. Job/Role Competencies Survey report.HR benchmark Group. Pittsburgh, PA: development Dimensions International 1998; 4(1).

[6] Cooper, Scott, Lawrence, Eton, Kierstead, James, Lynch, Brian, Luce, Sally. Competencies—A brief overview of development and application to public and private sectors. Ottawa: Public Service Commission of Canada, Research Directorate. Policy, Research and Communications Branch 1998.

[7] Draganidis, Mentzas. Competency Based Management; a review of Systems and approaches. Information Management & Computer Security 2006; 14(1):51- 64.

[8] Donzelli A, Walsh V. Introducing competency management at ESA. ESA Bulletin 2006; (ISSN 0376- 4265), 126:72 – 76.

[9] Ennis. Competency Models: A Review of the Literature and the Role of the Employment and Training Administration (ETA). U. S. Department of Labor 2008.

[10] Gangani McLean, Braden A. Competency-Based Human Resource Development Strategy. Performance Improvement Quarterly 2006; 19 (1): 127- 140.

[11] Greengard, Samuel. Make smarter business decisions: Know what employees can do. Workforce 2001; 80(11):42.

[12] Kumari A, Sita V. Role of Human competencies in Human Resource Management: A study in Indian organizations. OIDA International Journal Of Sustainable Development 2010; 2(3):29-34 Available at SSRN: http://ssrn.com/abstract=171037. 356 Kaushiki Tripathi and Manisha Agrawal

[13] Lepsinger L. The Art and sciences of competency models: pinpointing critical success factors in organization. San Francisco: Jossey- Bass/Pfeiffer 1999.

[14] McClelland. Testing for competence rather than intelligence. American Psychologist1973:1- 14.

[15] McClelland D.A Guide to Job Competency Assessment, McBer & Co., Boston, MA 1976. [16]

[16] McLagan P. Competencies: The Next Generation. Training & Development 1997: 40-47. [17]

[17] Ozcelik, Ferman. Competency Approach to Human Resource Management Outcomes and Contributions in a Turkish Cultural Context. Human Resource Development Review 2006; 5(1) :72-91

[18] Pickett, L. Competencies and managerial effectiveness: Putting competencies to work. Public Personnel Management 1998; 27(1):103–115.

[19] Rowe. Clarifying the use of competence and competency models in recruitment, assessment, and staff development. Industrial and commercial Training 1995; 27 (11):12-17

[20] Sparrow P. Organizational Competencies- a valid approach for the future. International Journal of Selection and Assessment 1995; 3(3):168-77.

[21] Spencer, Lyle M Jr, Spencer, Signe M. Competence at work. New York: Wiley 1993. [22] United Nations Industrial Development Organization. UNIDO Competencies. http://www.unido.org 2002.

International Journal of Management (IJM)
Volume 11, Issue 11, November 2020, pp. 4376-4382, Article ID: IJM_11_11_440
Available online at https://iaeme.com/Home/issue/IJM?Volume=11&Issue=11
ISSN Print: 0976-6502 and ISSN Online: 0976-6510
DOI: https://doi.org/10.17605/OSF.IO/P9HZJ

RSDQ MODEL OF 360 DEGREE FEEDBACK

Dr. Y Jayaprada
Research Scholar, Dr. A P J Abdul Kalam University, Indore, India;
Associate. Professor, Avanthi Institute of Engineering & Technology, Hyderabad, India

Dr. Sushil Beliya
Prof. Dr. A P J Abdul Kalam University, Indore, India

ABSTRACT

A large number of organizations have been using 360 degree feedback in India as leadership development intervention. This paper is based on the feedback of 43 participants from four companies where the 360 Degree Feedback program was initiated. The study was done using a questionnaire method. The results indicated that there has been an overall positive impact reported of 360 Degree intervention on ones professional life after 360DF. More than 60% of the participants report that they visited 360DF data every quarter. 24 participants reported that about 50% of their action plans prepared at the end of the 360 intervention were implemented. At least 30% of the action plans were achieved by 6 of the participants and 2 participants reported achievement of all their action plans. The participants also reported that the RSDQ model based 360DF tool provided detailed insight covering various parameters of one?s role. The participants also recommend that with more periodic follow up and review sessions (every quarter) anchored by internal HR and more focus and seriousness among the participants to work on the action plans will result in using 360 DF for change and growth.

Keywords: RSDQ, 360 Degree, Leadership, Management, HR, Feedback

Cite this Article: Dr. Y Jayaprada and Dr. Sushil Beliya, RSDQ Model of 360 Degree Feedback, International Journal of Management (IJM), 11(11), 2020, pp. 4376-4382. https://iaeme.com/Home/issue/IJM?Volume=11&Issue=11

INTRODUCTION

One of the most popular management and leadership development tools of recent times is 360 Degree Feedback. It is said that almost every fortune 500 organization uses 360 Degree. That 360 Degree Feedback is a cliche, is a cliché, and probably quite deserving of it, owing to the multiple purposes for which the instrument has been used in companies, Institutes, NGO s and even Schools! Vast has been its reach and coverage. Many organizations and most Not for Profit organizations have been found using 360DF as a leadership development tool.

While on one hand, India can boast about using the instrument across a range of companies and institutions; on the other, empirical research into the subject has been, if anything, very scanty, barely noticed or read about. Not very surprising, since India has primarily never been much into research implementing or publishing, both of which are done on a massive scale in the U.S as well as in Europe. While 360DF s reach across India is no small matter, we are still only a decade old though slowly but surely, maturing. Comforting news, that The RSDQ model (roles, styles, delegation, and qualities) was established by the TVRLS (T.V Rao Learning Systems) for top and senior management in terms of managerial and leadership competences required. Effective management and leadership are viewed as a mix of four sets of variables in this model of leadership and managerial effectiveness.

Roles: How much a person participates in various leadership and management jobs and activities. To be effective as a manager, every manager must take on a variety of responsibilities. These roles encompass both transformative (leadership) and transactional (management) tasks, such as:

- Customer management on the inside.
- Customer management from the outside.
- Organizing and managing unions and groups.
- Managing and introducing new technology and systems.
- Juniors must be inspired, developed, and motivated.
- Taking charge of juniors, coworkers, and seniors.
- Articulating and sharing one's values and vision.
- Developing policies and plans for the long term.
- Culture building.

Styles: While effective managers recognize and execute leadership duties, it is not just the positions or activities that define effectiveness, but also how they are executed. The model assumes that managers can perform well in most positions, spend time and effort, but are unconcerned about the manner in which they carry out these tasks. The author has categorized the leadership styles into the following categories based on previous study at the Indian Institute of Management:

A paternalistic or benevolent leadership style in which the top management believes that all of his employees should be continually supervised and treated with affection, as if they were his children. It prioritizes relationships, assigns jobs based on his own preferences, continually leads and protects them, recognizes their requirements, aggressively intervenes in crisis situations to save them, rewards loyal and obedient employees, and shares information with people closest to him.

A critical leadership style is similar to the Theory X belief pattern, in which the manager believes that employees should be closely supervised, directed, and reminded of their duties and responsibilities on a regular basis, in short-term goal-oriented, cannot tolerate mistakes or conflicts among employees, personal power dominated, keeps all information to himself, and works strictly according to norms and rules.

A developmental leadership style is defined as an empowering style in which the top manager believes in developing his employees' competencies, treats them as mature adults, leaves them on their own the majority of the time, is long-term goal oriented, shares information with all to build their competencies, and facilitates conflict and mistake resolution by the employees themselves.

The developmental form of organization construction has been discovered to be the most popular. However, some people and situations necessitate benevolent and critical methods at different times. According to research, some managers are unaware of their dominating management style or the impact it has on their workforce.

Delegation: The RSDQ model regards a senior executive's ability to delegate as a significant factor in their effectiveness. This component was introduced since most senior managers, especially the competent managers who advance quickly in their careers, appeared to have difficulty delegating. As a result of these experiences, delegation has been identified as a critical leadership variable. Those who delegate free up time to focus on higher-level activities, while those who don't continue to handle lower-level activities, stifling their leadership and managerial effectiveness.

Qualities: Managers should have attributes of leaders and world-class managers, according to the model (for example, pro activity, listening, communication, positive approach, participative character, and quality orientation). Such attributes have a significant impact on the efficacy with which top-level managers perform diverse jobs, as well as on leadership style, and are thus quite important.

The RSDQ model is used to create the TVRLS 360-degree feedback instrument for managerial and leadership development. There are around 75 actions recognized under each of the jobs stated above in terms of managerial skills. An instrument was designed to assess the extent to which the manager is seen to be executing these duties (two versions: one with 55 items for senior managers and the other with 75 items for top level managers).A 51-item instrument evaluates the extent to which the aforementioned styles are displayed in 12 different situations or activities, as well as the impact the person has on his subordinates in terms of five variables: feelings (dependence, incompetence, independence, interdependence, and resentment), job satisfaction, work commitment, morale, and extent of learning. The participant learns about his benevolent, critical, or developmental (dominant and backup) styles, as well as their influence, using this instrument. The delegation questionnaire determines how much time the participant is delegating and releasing for higher-level jobs and responsibilities. A ten-item questionnaire assesses the various symptoms of delegation and non-delegation. In the instance of behavioral traits, the semantic differential approach is now used to incorporate 25 attributes. Three open-ended questions in the end attempt to elicit the respondent's most prominent qualities and faults, as well as suggestions for development.

With changes in their business environment, the instruments established on the basis of the RSDQ model are updated on a regular basis based on characteristics crucial to top management responsibilities and positions.

INDIAN ORGANIZATIONS AND 360 DEGREE FEEDBACK

Although a well-established concept in the West, 360-degree feedback is gradually gaining acceptance in Indian organizations.

Objective of 360- degree feedback

- In most cases, 360-degree feedback is being used as a developmental tool. Only 1 out of 9 organizations use it for promotions and rewards.

Coverage

- 7 out of 9 organizations use it for their top management. 1 of the 9 organizations provided the feedback on a voluntary basis

Parameters on which feedback is sought

The most common dimensions on which feedback is sought are:

- Ownership
- Commitment to excellence
- Communication
- Initiative
- Team skills
- Commitment
- Customer orientation
- Learning

Role of HR Department

The HR department was found to perform one or many of the roles enlisted below:

- Promoting the concept through orientation workshops
- Acting as the coordinating body, finalizing list of assessors, sending the questionnaires, etc.
- Compiling the feedback and preparing the profile
- Liaising with the external agency in preparing the feedback profiles
- Conducting counseling sessions and reviewing development post- 360 -degree feedback

Objectives:

1.To put RSDQ model of 360DF under the scanner (so to speak), and thereon

2. To find if the 360Degree Feedback can correctly identify star performers, differentiating them from other average and low performers, and

3. To authenticate 360DF s results opposed to some other method of identifying performers

or stars, i.e. through the common Performance Appraisal system; and finally,

4. To document a conceptual framework, outlining integration of research findings with practical application and providing possible direction for future value adding utility. Target Population who will find the study and outcomes useful are all Managers, Executives, Consultants, Institutes and any type of organization members. There is the hope that such type of study will influence researchers and managers to delve more deeply into the area of 360 Degree Feedback. Charting an unexplored ocean, if you will!!

Focus of this study has been on organizations, but as a tool, 360DF has been implemented in institutions, be they commercial or otherwise, and even schools. As a consultant, the most comforting and redeeming part of the exercise has been the experience of working with schools i.e. school teachers, Principals, their trustees and other such staff who have gone through the feedback process. We have also successfully managed to apply the same to PG students doing their MBA. It is quite fascinating to see one common instrument, the 360DF, being sculpted to suit various audiences needs. The process essentially remains the same. What changes is the Questionnaire, its dimensions and variables on which feedback is sought.

Any study always has certain assumptions kept in mind while creating the tool/instrument. This study is no different, the assumption here being that Performance Appraisal method is correct and valid, providing correct results (Performance based Pay, Rewarding those deserving)

NEED FOR THE STUDY

The theme has the element of 360Degrfee Feedback, a concept which is, relatively speaking, new in our country. Similarly, the very idea of identifying individuals and putting them on a fast track (system and process catering to identifying future leaders and grooming them for future roles) is itself less than a decade old (India). Both these concepts and tools are recently being used by a multitude of organizations. While the nuances of 360DF and Fast Track Performers will vary from company to company, the fundamental concepts, purpose for using them and the result will essentially be the common thread providing the linkage of one with another.

The latest need on the block is Retention, or rather, prevention of high employee attrition which most companies today face. Given the rate of Globalization and change, companies are extending efforts to give performers better incentives by inflating their egos and hooking them into a very well laid out scheduled career path that is full of royal treatment along the way to becoming king! Needless to say, such schemes or plans, if left in between, will mean the individual having to start from scratch establishing his credentials and performance potency. Which in turn implies lost time that the HR manager hope will not be worth the change for the intending candidate and that s how current retention programs are in the limelight.

ABRIEF REVIEWOF 360 DEGREE FEED BACK

"The (360 degree) feedback process...involves collecting perceptions about a person s behavior and the impact of that behavior from the person s boss or bosses, direct reports, colleagues, fellow members of project teams, internal and external customers, and suppliers. Other names for 360 degree feedback are multi-rater feedback, multi-source feedback, full-circle appraisal, and grouper formance review". describes 360 Degree feedback as the systematic collection and feedback of performance data on an individual or group, derived from a number of the stakeholders in their performance. Assessment through 360 Degree feedback is normally via a questionnaire completed by a stakeholder in the individual s performance: those who work closely enough with the manager to respond to questions about their behavior and its impact. The data is then fed back to the participant, in a way that is intended to result in acceptance of the information and the formulation of a development plan The 360 Degree feedback seems to be so powerful that even the cabinet secretariat of the U.K. has introduced 360 degree Feedback to increase self awareness of Civil servants. The underpinning assumption for this development was that a key criterion for good leadership is self-awareness (Cabinet Office) and that if done well, it is a very powerful tool of management and a very good way of helping people improve their own performance Perhaps the most notable work on perceptions of managers to 360 Degree feedback in a UK context was a study by *Mabey*. He examined managers reactions at the Open University during 360 Degree feedback process implementation. This study established that many managers perceived that they had not developed a particularly different understanding of themselves, but the process had reinforced the direction of their development. Interestingly, as Mabey (2001) notes, in contrast to assumptions made by other commentators, some participants suggested the process would gain more if results were not private as their accountability to act might be increased. Yet the availability of individual results might increase what McCauley and *Moxley)* call the approach avoidance reaction to feedback, meaning that managers may wish to understand the perceptions of those around them, yet may be concerned about hearing their weaknesses and try to control the possibility of negative feedback. Despite numerous positive descriptions of the potential benefits of 360 Degree feedback, some studies give reason to question whether any real development actually occurs, or whether the process is as positive an experience as suggested However, in terms of growing commitment to the system *Waldman and Bowen (1998)* indicate this is more likely to improve with time.

This is because managers become more assured of senior management commitment and their intentions surrounding the process become clearer

CONCLUSION

360-degree appraisal and feedback mechanisms are being used in various organizations. A common belief is that an organization needs special instruments designed for such an appraisal before any such appraisal can be implemented. On the contrary, a large number of instruments available to measure individual behavior can be modified very quickly for 360-degree appraisal.

- It is not always necessary to get instruments specially designed for 360-degree appraisal. You can easily adapt any existing instrument that you may be familiar and comfortable with. That gives you a wider range of instruments to be used for such a purpose.
- The instrument does not have to be of an appraisal type. The above experience shows that an instrument for self-development could be used just as effectively to get more insight into one's behavior.
- The organization need not take initiative for 360-degree appraisal. The individual may take his or her own initiative. The organization would go in for such a feedback once they see the success of such a mechanism.
- The dependency on foreign instruments for 360-degree feedback can be reduced since there are hundreds of Indian instruments available, which may be used for such a purpose.

REFERENCES

[1] Neharika Vohra, and Manjari Singh, Mental traps to avoid while interpreting feedback: Insights from administering feedback to school Principals, Human Resources Development Quarterly, 2005, 16(1), 139-147.

[2] Rai, Himanshu and Singh, Manjari, Mediating Effects in the Relationship between 360- Degree Feedback and Employee Performance, Ahmadabad: Indian Institute of management, Working Papers, 2005 (W.P. No. 2005-04-06)

[3] Rao, T. V, and Annapurna, J. An exploratory study of changes in the roles and competencies of top-level managers due to 360-degree feedback, Ahmadabad: Unpublished research Paper

[4] Rao, T. V. and Chawla, Nandini 360 Degree feedback and Assessment and Development Centres, New Delhi: Excel Publications, 2005

[5] Rao, T. V. and Rao, Raju, 2003 The Power of 360 Degree Feedback, New Delhi: Sage Response Books.

[6] Rao, T. V. Mahapatra, G, Rao, Raju and Chawla, Nandini. 360 Degree feedback and Performance management Systems, New Delhi: Excel Publications, 2002

[7] Rao, T. V. Vijayalakshmi, M and Rao, Raju: 360 Degree feedback and performance Management Systems, New Delhi: Excel Publications, 2000

[8] Antonioni, D. (1996). Designing an effective 360-degree appraisal feedback process. Organizational Dynamics.

[9] Atwater, L., & Waldman, D. (1998). 360 degree feedback and leadership development. Leadership Quarterly, 423-426.

[10] Bracken, D. W., & Rose, D. S. (2011). When does 360-degree feedback create behavior change? Journal of Business and Psychology, 183-192.

[11] Carson, M. (2006). Saying it like it isnt: The pros and cons of 360-degree feedback. Business Horizons, 395-402.

[12] Edwards, M. R., & Ewen, A. J. (1996). Review of 360-degree feedback: The powerful new model for employee assessment & performance improvement. American Management Association.

[13] Goldschmidt, Pequeriaux, & Jongh-Leuvenink. (2002). The quality of leadership (QL): The EFQM leadership criterion in relation to the 360-feedback evaluation method. Accreditation and Quality Assurance, 468-472.

[14] Journal of Personality and Social Psychology, 36, 1202-12.

[15] Sperry, Len & L.R. Hess (1974), Contract counseling, Addition Wesley, Reading, Mass.

[16] Starling, G. (1982). Performance Appraisal in the Z organization, Public Personnel Management Journal, 11(4), 343-51.

[17] Thornton, G.C.& W.C. Byham (1982). Assessment centers and Managerial performance, Acadamic Press, New York.

[18] Tornow, W.W, M.London & CCI Associates (1998). Maximising the value of 360

[19] Degree Feedback, Jowwey-Bass Ibc.

[20] Tversky, A, & D. Kahneman (1974). Judgement under Uncertainty: Henristics and Biases, Science,185,1124-31.

[21] Warmke, D.L.&R.S.Billings (1979). Comparison of Training Methods for improving the Psycho-Metric Quality of Experimental and Administrative performance Rating, Journal of Applied Psychology,124-31.

[22] Yakavac, M. (996). Paying for Satisfaction, HR Focus, June, pp.10-11.

JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 7, ISSUE 01, 2020

Performance Analysis and Practices

Author1: Dr. Y Jayaprada
Author2: Dr. Sushil Beliya

Abstract – According to recent studies, the dairy sector has placed a large emphasis on its human resource for many decades because it is the most valuable and valuable resource. The performance analysis in this study looked at four functions to assess the competitiveness of the dairy sector's Human Resources

Key words: HR Management, Training, employee participation

1. INTRODUCTION

People are always in demand, but unlike finance, they cannot be simply replaced by technology or transferred about. To ensure that a dairy company's manpower capital is made up of the right people, in the right place, at the right time, to produce high-quality value for business capital in conjunction with communities, a systematic approach to applying human resource practice is required.

Many HR writers have regarded and described human resources as an organization's most valuable asset. People differ in every way, despite their complex and dynamic nature, which includes their personality, character, and ability to attain goals.

1. Recruitment and Selection
2. Training and development
3. Performance Management System
4. Compensation and Benefits

While recruiting prospects, firms should carefully map the available HR because they provide a competitive advantage for the company. The organization must look at the candidate's competency area and provide relevant training to them while training them. The primary goal of training is to increase the performance of dairy industry human resources. Compensation and benefits are a crucial factor in a company's recruiting rate, retention rate, and overall employee satisfaction. Due to the entry of global firms, dairy companies are improving modern HR methods.

The purpose of this article is to investigate the Human Resource Practices of Mother Dairy Private Limited, which is currently regarded as the best firm in the Indian dairy industry as a whole. The availability of excellent HR practices in firms makes them competitively advantageous, as well as supporting the organizations' genuine people.

The objective of this research is to conduct a literature evaluation on HR practices used in businesses. Both primary and secondary data were used in the study. The primary data was acquired from 34 Mother Dairy employees using an offline questionnaire, and the findings were calculated using the percentage technique. According to the findings, Mother Dairy Fruits & Vegetables Private Limited follows standard HR Practices and their employees are content with the organizational climate, indicating that their company follows an ethical HR policy.

ISSN- 2394-5125 VOL 7, ISSUE 01, 2020

Recruitment is the most fundamental function of HR: it is the process of finding employees to apply for job openings at Mother Dairy Private Limited. The selection process, on the other hand, is the procedure for selecting the best candidate from a pool of applicants gathered by recruiting. After the recruitment procedure, the selection procedure takes place.

Once an employee joins the company, he or she is trained and developed in accordance with the company's needs and project areas. Once an employee has been trained, he or she performs, and based on their performance and appraisal analysis, a decision is made about remuneration and payment.

For large firms, the HR practices procedure will be lengthy, while for dairy firms, the procedure will be more extensive, and it will differ from one industry to the next. Many variables must be considered when following HR practices, for example, when selecting a candidate, the best HR activities must be chosen from aptitude testing, group discussions, work history, and referral history.

Performance appraisal methods and procedures in some Asian nations are comparable to those in India. However, other systems, such as those in Japan, have grown over time to become essential components of the Japanese management philosophy and style. As in India, performance rating systems in Singapore, Malaysia, the Philippines, Pakistan, Indonesia, and Sri Lanka are a mixed bag. The purpose of this chapter is to illustrate some of the significant developments in some of these countries. The fundamental argument of this chapter is that, in comparison to other Asian countries, Indian businesses are probably slightly better off in terms of the appraisal systems they have or are experimenting with (if we do not consider the multinational present in these countries whose appraisal systems are decided largely by their western Counterparts.).Because most of these countries lack well-established institutions for doing management research, the available literature is sparse. For example, in the previous several years, there have been only one or two publications on this issue published in Singapore's major publications (for example, Singapore Institute of Management).However, countless papers, articles, and workshop summaries have appeared in local journals as a result of the spike in public interest in assessment systems in Singapore over the previous two years. These sources were used to make the observations in this chapter. Additional material was obtained from the author's trips to several of the institutes in the Philippines, Malaysia, and Singapore, as well as meetings with professional colleagues from these and other countries. Finding research and case studies on Asian countries' performance assessment methods remained difficult even in places like the Philippines, where the Asian Institute of Management existed. This, in and of itself, reflects the current state of evaluations as well as managers' and the management profession's past disregard of this subject. Western management literature, on the other hand, has paid some attention to this topic. For example, their Journal of Applied Psychology has had at least one article dealing with appraisal-related themes in each of the last three years.

Research objective:

The main purpose of the study was to identity the impact of HR practices on competitiveness of the dairy sector's

ISSN- 2394-5125 VOL 7, ISSUE 01, 2020

Training and Employee development:

Training is done to create change by initiating a new employee into the culture of the organization. It involves new employees acquiring new skills or improving their skills in order to implement change that is needed by an organization. Training is not sufficient enough to motivate work force. But, it is an important tool that an organization can use to achieve its long term goals (Laird, Holton III, & Naquin, 2003). ISSN: 2289-4519 Page 32 Training given to employees is done as an agreement to maintain culture of the organization and also to be productive which in turn will result in earning reward and awards. Training also plays an important role in employee performance as the skills acquired during the training will be the major part of the employee life-cycle in an organization. Training as a tool will help an employee to upgrade his knowledge and technicality and improves his performance in the organization. Training plays an important role in motivating employees to take part in organized projects, to willingly support programs that will improve the organization and to do their best in order to see that organizational goals are achieved (Bolman & Deal, 2011).

Performance Appraisal:

Performance appraisal is used by organizations to evaluate employees' efforts so as to reward them for the efforts. Performance appraisal was found to have both direct and indirect effect on administrative performance of employee and the feedback obtained from performance appraisal activities, usually conducted at least once annually can help to improve administrative processes.

Limitations and future study:

There are also many limitations of this study which includes; First, the study is only limited to a single telecom major in Malaysia, So the results of this study can only be used for further research in telecom industry at different levels. Secondly the HR practices discussed in this study are very short in numbers. These HR practices are taken from the research work already done by different researchers and according to the predominant HR practice at Telekom Malaysia, hence there are several other practices which could be focused in future studies.

References:

Ahmad, S., & Schroeder, R. G. (2003). The impact of human resource management practices on operational performance: recognizing country and industry differences. Journal of Operations Management, 21(1), 19-43.

Bae, J., & Lawler, J. J. (2000). Organizational and HRM strategies in Korea: Impact on firm performance in an emerging economy. Academy of Management Journal, 43(3), 502-517.

BARNEY, J., & Hesterly, W. (2006). 1.3 Organizational Economics: Understanding the Relationship between Organizations and Economic Analysis. The SAGE handbook of organization studies, 111.

Becker, B. E., & Huselid, M. A. (2006). Strategic human resources management: where do we go from here? Journal of management, 32(6), 898-925.

Bharadwaj, A. S. (2000). A resource-based perspective on information technology capability and firm performance: an empirical investigation. MIS quarterly, 169- 196.

ISSN- 2394-5125 VOL 7, ISSUE 01, 2020

Bolman, L. G., & Deal, T. E. (2011). Reframing organizations: Artistry, choice and leadership: Jossey-Bass.

Bowen, D. E., & Ostroff, C. (2004). Understanding HRM–firm performance linkages: The role of the "strength" of the HRM system. Academy of management review, 29(2), 203-221.

Cardon, M. S., & Stevens, C. E. (2004). Managing human resources in small organizations: What do we know? Human resource management review, 14(3), 295-323.

Carlson, D. S., Upton, N., & Seaman, S. (2006). The Impact of Human Resource Practices and Compensation Design on Performance: An Analysis of Family-Owned SMEs. Journal of Small Business Management, 44(4), 531-543.

Castilla, E. J. (2005). Social Networks and Employee Performance in a Call Center1. American Journal of Sociology, 110(5), 1243-1283.

Collins, C. J., & Clark, K. D. (2003). Strategic human resource practices, top management team social networks, and firm performance: The role of human resource practices in creating organizational competitive advantage. Academy of Management Journal, 46(6), 740-751.

Collins, C. J., & Smith, K. G. (2006). Knowledge exchange and combination: The role of human resource practices in the performance of high-technology firms. Academy of Management Journal, 49(3), 544-560.

Combs, J., Liu, Y., Hall, A., & Ketchen, D. (2006). How much do high-performance work practices matter? A meta-analysis of their effects on organizational performance. Personnel Psychology, 59(3), 501-528.

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2

RESEARCH ARTICLE OPEN ACCESS

A MPPT ALGORITHM BASED PV SYSTEM CONNECTED TO VOLTAGE CONTROLLED GRID

Y. DEEPIKA[1] E. PRASANNA[2]
[1] PG Student, [2]Asst. Professor
AVANTHI INSTITUE OF ENGINEERING & TECHNOLOGY

ABSTRACT

Future ancillary services provided by photovoltaic (PV) systems could facilitate their penetration in power systems. Also low power PV systems can be designed to improve the power quality. This paper presents a single-phase photovoltaic system that provides grid voltage support and compensation of harmonic distortion at the point of common coupling (PCC) thanks to a repetitive controller. The power provided by the PV panels is controlled by a Maximum Power Point Tracking (MPPT) algorithm based on the incremental conductance method specifically modified to control the phase of the PV inverter voltage. Simulation validate the presented solution.

Index Terms: Maximum Power Point Tracking (MPPT) algorithm, shunt controller, single-phase photovoltaic (PV) inverter.

1.1 Introduction to the Project

Among the renewable energy sources, a noticeable growth of small photovoltaic (PV) power plants connected to low-voltage distribution networks is expected in the future. As consequence, research has been focusing on the integration of extra functionalities such as active power filtering into the PV inverter operation. Distribution networks are less robust than transmission networks, and their reliability, because of the radial configuration, decreases as the voltage level decreases. Hence, usually, it is recommended to disconnect low-power systems when the voltage is lower than 0.85 pu or higher than 1.1 pu . For this reason, PV systems connected to low- voltage grids should be designed to comply with these requirements but can also be designed to enhance the electrical system, offering "ancillary services". Hence, they can contribute to reinforce the distribution grid, maintaining proper quality of supply that avoids additional investments. However, low-voltage distribution lines have a mainly resistive nature, and when a distributed power generation system (DPGS) is connected to a low-voltage grid, the grid frequency and grid voltage cannot be controlled by independently adjusting the active and reactive powers. This problem, together with the need of limiting the cost and size of DPGS, which should remain economically competitive even when ancillary services are added, makes the design problem particularly challenging. This paper proposes to solve this issue using a voltage controlled converter that behaves as a shunt controller, improving the voltage quality in case of small voltage dips and in the presence of nonlinear loads.

Shunt controllers can be used as a static var generator for stabilizing and improving the voltage profile in power systems and to compensate current harmonics and

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

unbalanced load current . In this paper, the PV inverter not only supplies the power produced by the PV panels but also improves the voltage profile, as already pointed out. The presented topology adopts a repetitive Controller that is able to compensate the selected harmonics. Among the most recent Maximum Power Point Tracking (MPPT) algorithms, an algorithm based on the incremental conductance Method has been chosen. It has been modified in order to take into account power oscillations on the PV side, and it controls the phase of the PV inverter voltage.

Renewable energy sources like wind, sun, and hydro are seen as a reliable alternative to the Traditional energy sources such as oil, natural gas, or coal. Distributed power generation systems (DPGSs) based on renewable energy sources experience a large development worldwide, with Germany, Denmark, Japan, and USA as leaders in the development in this field. Due to the increasing number of DPGSs connected to the utility network, new and stricter standards in respect to power quality, safe running, and islanding protection are issued. As a consequence, the control of distributed generation systems should be improved to meet the requirements for grid interconnection. This paper gives an overview of the structures for the DPGS based on fuel cell, photovoltaic, and wind turbines. In addition, control structures of the grid-side converter are presented, and the possibility of compensation for low-order harmonics is also discussed. Moreover, control strategies when running on grid faults are treated. This paper ends up with an overview of synchronization methods and a discussion about their importance in the control.

2. VOLTAGE AND FREQUENCY SUPPORT

2.1 Overview

The power transfer between two sections of the line connecting a DPGS converter to the grid can be studied using a short line model and complex phasors, as shown in Fig.2.1. When the DPGS is connected to the grid through a mainly inductive line X>> *R*, *R* may be neglected. If the power angle δ is also small, then

$$\sin\delta \cong \delta \; and \; \cos\delta \cong 1 \text{ and}$$

$$\delta \cong \frac{XP_A}{V_A V_B} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V_A - V_B \cong \frac{XQ_A}{V_A} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where V_A, V_B, Q_A and denote, respectively, the voltage, active power, and reactive power in section A, and V_B is the voltage in section B, as indicated in Fig.2.1

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

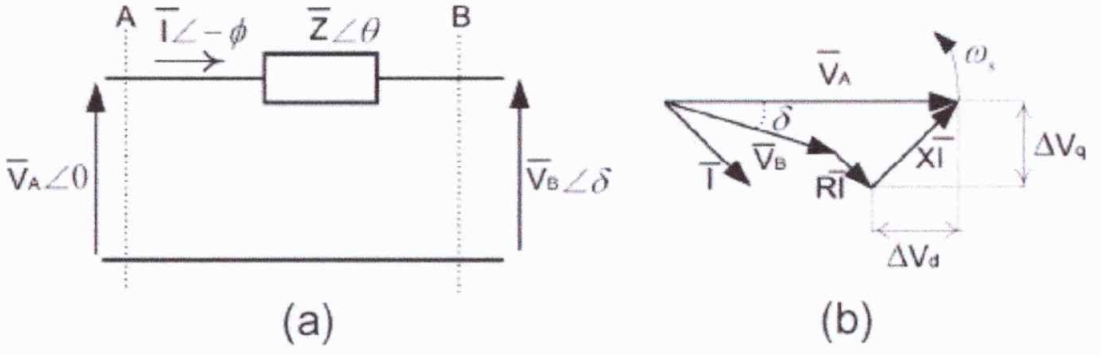


Fig 2.1 a) power flow through a line **b) Phasor Diagram**

For X_R, a small power angle δ, and a small difference V_A, V_B, equations (1) and (2) show that the power angle predominantly depends on the active power, whereas the voltage difference V_A, V_B predominantly depends on the reactive power. In other words, the angle δ can be controlled by regulating the active power, whereas the inverter voltage V_A is controlled through the reactive power. Thus, by independently adjusting the active and reactive powers, the frequency and amplitude of the grid voltage are determined. These conclusions are the basis of the frequency and voltage droop control through active and reactive powers, respectively [7]. In this paper, the relation (1) has been adopted to optimize the power extraction from PV panels (MPPT).

2.2 Shunt Controllers For Voltage Dip Mitigation

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

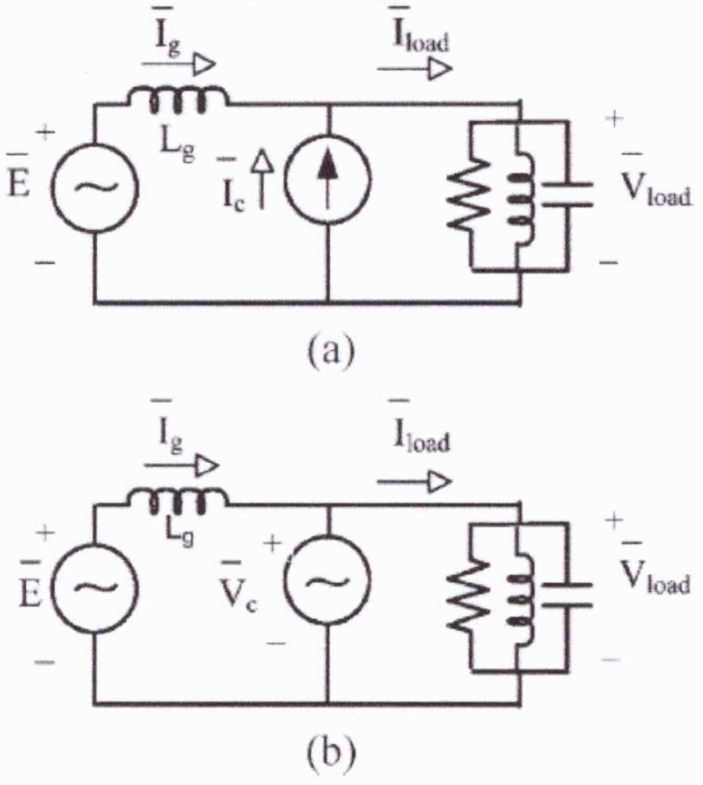
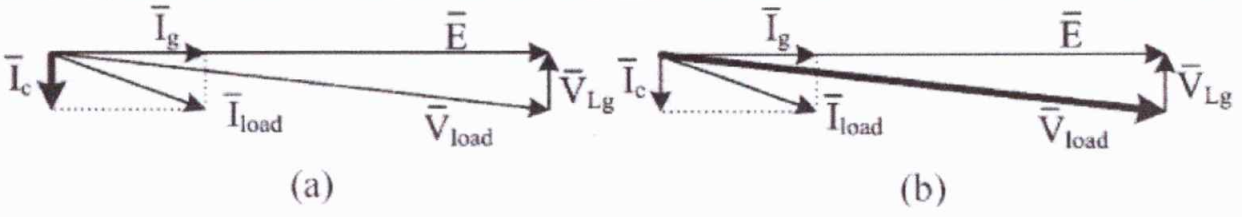


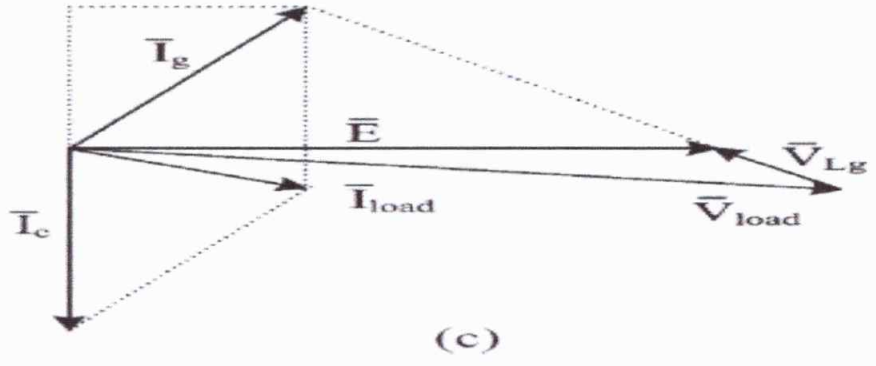
Fig 2.2. Use of a shunt controller for voltage dip compensation.
(a) Simplified power circuit of the current-controlled shunt controller.
(b) Simplified power circuit of the voltage-controlled shunt controller.

Shunt devices are usually adopted to compensate small voltage variations that can be controlled by reactive power injection. The ability to control the fundamental voltage at a certain point depends on the grid impedance and the power factor of the load. The compensation of a voltage dip by current injection is difficult to achieve because the grid impedance is usually low and the injected current has to be very high to increase the load voltage. The shunt controller can be current or voltage controlled. When the converter is current controlled, it can be represented as a grid-feeding component [Fig. 2.1(a)] that supports the grid voltage by adjusting its reactive output power according to the grid voltage variations. When the converter is voltage controlled, it can be represented as a grid-supporting component [Fig. 2.1(b)] that controls its output voltage ,however also in this second case, the control action results in injecting the reactive power in order to stabilize the voltage. The vector diagrams of a shunt controller designed to provide only reactive power are reported in Fig.2.3. When the grid voltage is 1 pu, the converter supplies the reactive power absorbed by the load, and the vector diagram of the current- or voltage-controlled converter is the same, then, in the first case, it is controlled by the compensating current I_c,and in the second one, it is controlled by the load voltage, as underlined in Fig.2.3(a)and (b).

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS



(a) Current-controlled converter b) Voltage-controlled converter in normal condition.



(c) Vector diagram for compensation of a voltage dip of 0.15 pu.

Fig.2.3. Vector diagram of the shunt controller providing only reactive power.

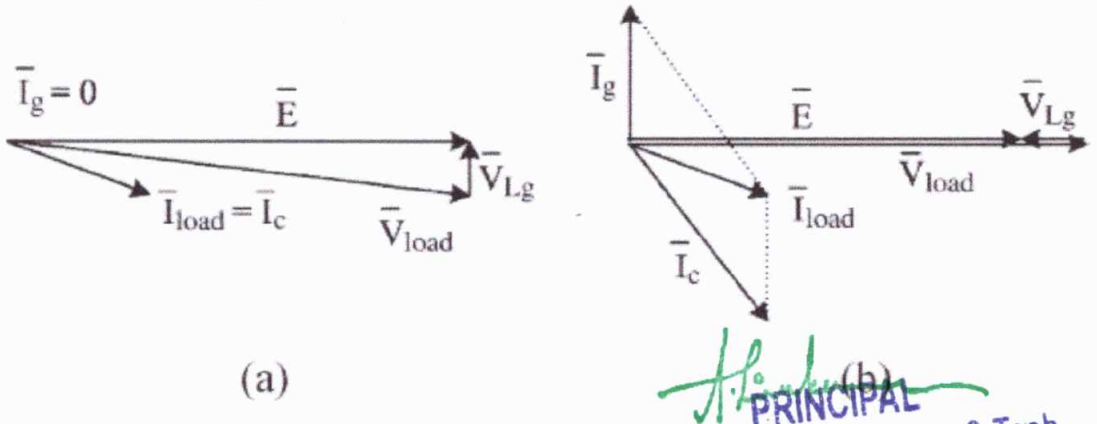


Fig.2.4 Vector diagram of the shunt controller providing both active and reactive powers. (a) Normal conditions. (b) Vector diagram for compensation of a voltage dip of 0.15 pu.

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

When a voltage sag occurs, the converter provides reactive power in order to support the load voltage, and the grid current I_g has a dominant reactive component,

i.e.,

$$I_g + I_C = I_{load} \quad \text{.....(3)}$$

The amplitude of the grid current depends on the value of the grid impedance since

$$I_g = \frac{V_{L_g}}{j\omega L_g} \quad \text{.....(4)}$$

Where V_{L_g} is the inductance voltage drop shown in Fig.2.3(c).If the shunt controller supplies the load with all the requested active and reactive powers, in normal conditions, it provides a compensating current $I_C = I_{load}$; hence, the system operates as in island mode, and $I_g = 0$. In case of a voltage dip, the converter has to provide the active power required by the load, and it has to inject the reactive power needed to stabilize the load voltage, as shown in Fig.2.4(b). The grid current in this case is reactive. It can be seen that

$$V_{load} = \text{E} + V_{L_g} \quad \text{..... (5)}$$

Hence, during a voltage sag, the amount of reactive current needed to maintain the load voltage at the desired value is inversely proportional to ωLg. This means that a large inductance will help in mitigating voltage sags, although it is not desirable during normal operational operation.

3. PV SYSTEM WITH SHUNT CONNECTED MULTIFUNCTIONAL CONVERTER

In case of low-power applications, it can be advantageous to use the converter that is parallel connected to the grid for the compensation of small voltage sags. This feature can be viewed as an ancillary service that the system can provide to its local loads. The proposed PV converter operates by supplying active and reactive powers when the sun is available. At low irradiation, the PV converter only operates as a harmonic and reactive power compensator. It is difficult to improve the voltage quality with a shunt controller since it cannot provide simultaneous

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

control of the output voltage and current. In addition, a large-rated converter is necessary in order to compensate voltage sags.

However, this topology is acceptable in PV applications since the PV shunt converter must be rated for the peak power produced by the panels. In the proposed system, the PV converter operates as a shunt controller; it is connected to the load through an LC filter and to the grid through an extra inductance L_g of 0.1 pu, as shown in Fig.5.1.usually, in case of low-power applications, the systems are connected to low-voltage distribution lines whose impedance is mainly resistive. However, in the proposed topology, the grid can be considered mainly inductive as a consequence of Lg addition on the grid side. However, since the voltage regulation is directly affected by the voltage drop on the inductance Lg, it is not convenient choosing an inductance Lg of high value in order to limit the voltage drop during grid normal conditions. It represents the main drawback of the proposed topology.

3.1 Control Of Converter

The proposed converter is voltage controlled with a repetitive algorithm. An MPPT algorithm modifies the phase displacement between the grid voltage and the ac voltage produced by the converter in order to force it to inject the maximum available power in the given atmospheric conditions. Hence, current injection is indirectly controlled. The amplitude of the current depends on the difference between the grid voltage and the voltage on the ac capacitor V_c .The phase displacement between these two voltages determines the injected active power (decided by the MPPT algorithm), and the voltage amplitude difference determines the reactive power exchange with the grid. The injected reactive power is limited by the fact that a voltage dip higher than 15% will force the PV system to disconnect (as requested by standards). The active power is limited by the PV system rating and leads to a limit on the maximum displacement angle $d\delta$ mppt. Moreover, the inverter has its inner proportional integral (PI)-based current control loop and over current protections.

3.2 Main Blockdiagram

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

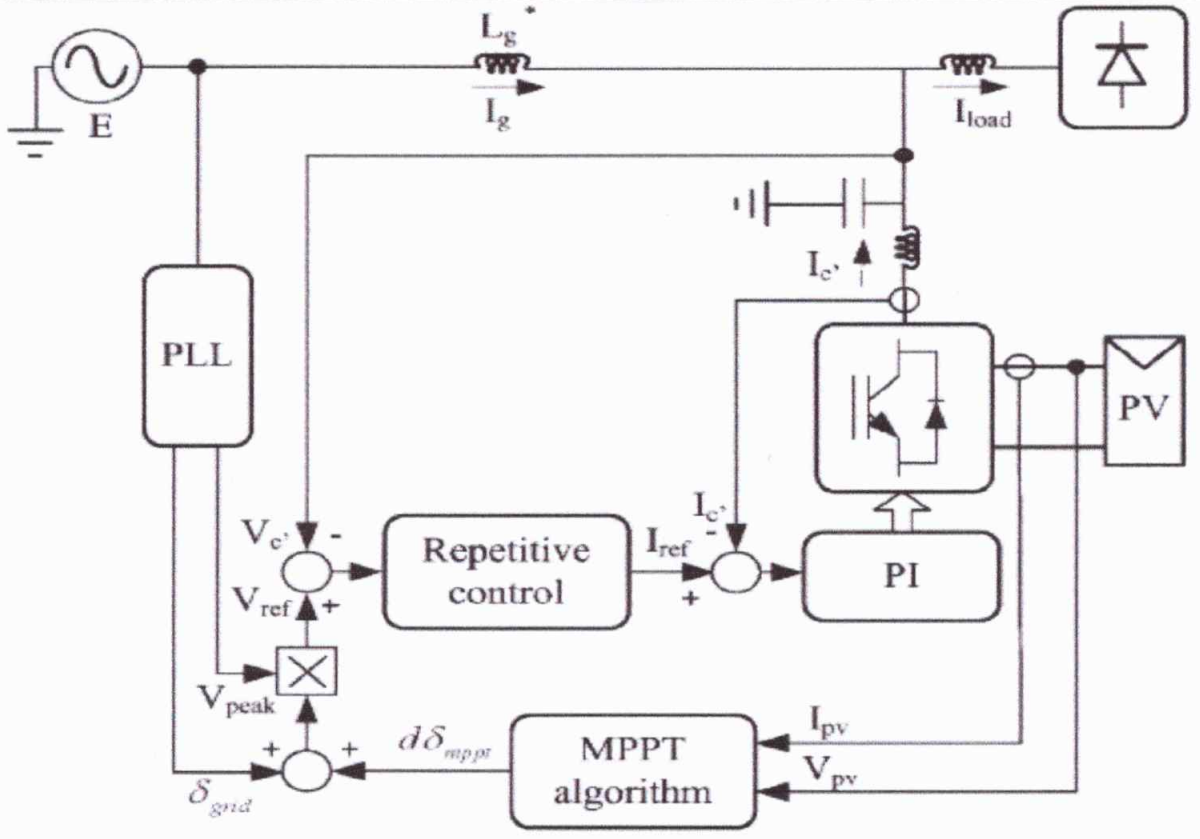


Fig 5.1 Grid connected PV system with shunt controller functionality

The voltage error between V_{ref} and V_c is preprocessed by the repetitive Controller, which is the periodic signal generator of the fundamental component and of the selected harmonics In this case, the third and fifth ones are compensated (Fig.5.3).

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

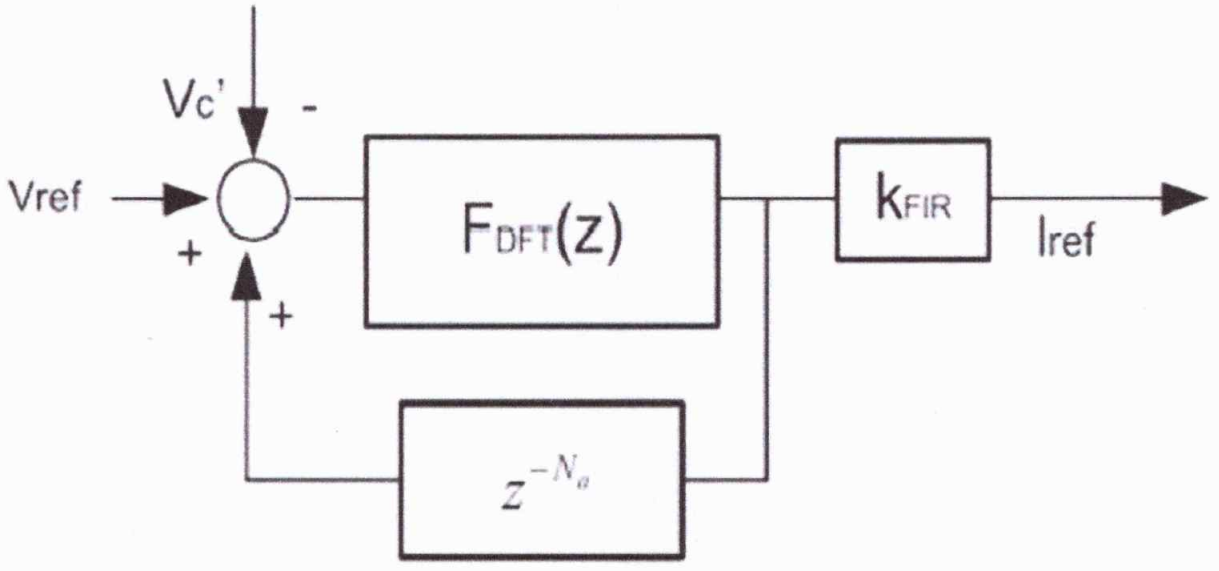


Fig.5.2 Control scheme

The proposed repetitive controller is based on a finite impulse response (FIR) digital filter [20]. It is a "moving"or "running" filter, with a window equal to one fundamental.

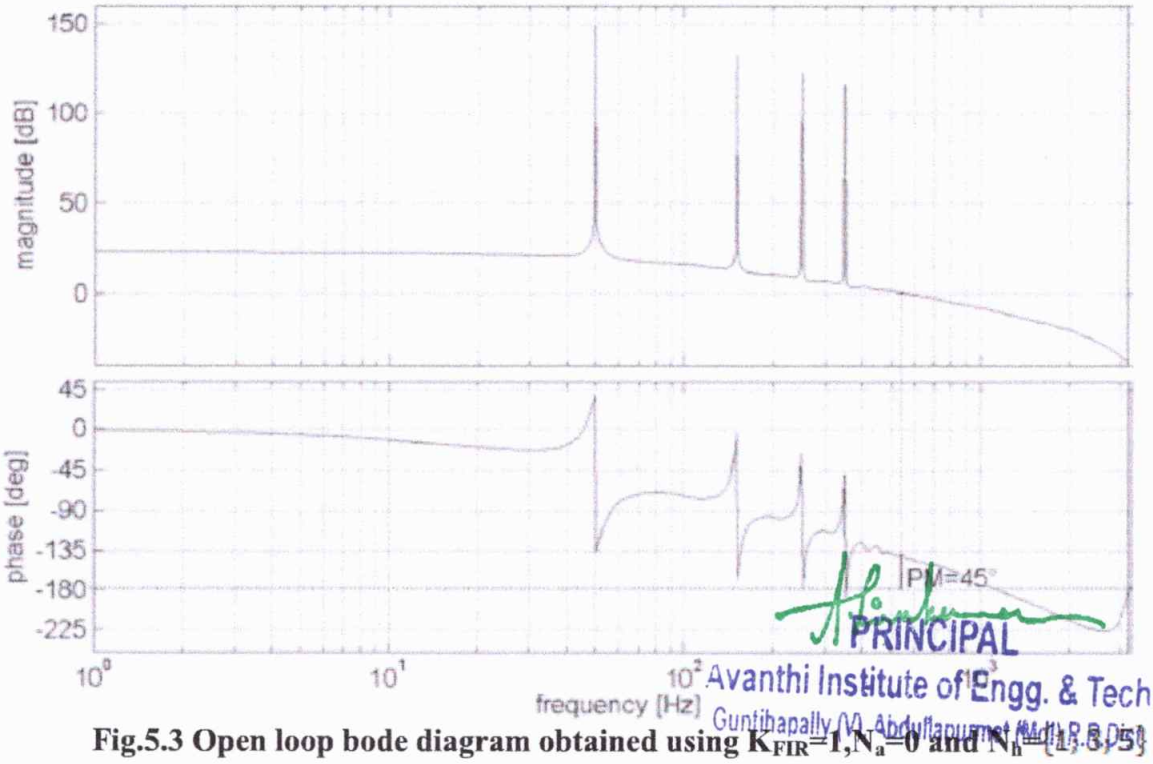


Fig.5.3 Open loop bode diagram obtained using K_{FIR}=1,N_a=0 and N_h=[1, 3, 5]

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

$$F_{DFT}(Z) = \frac{2}{N} \sum_{i=0}^{N-1} \left(\sum_{h \in N_h} cos \left[\frac{2\pi}{N} h(i + Na) \right] \right) . z^{-i} \quad \text{..... (6)}$$

where N is the number of samples within one fundamental period, N_h is the set of selected harmonic frequencies, and N_a is the number of leading steps determined to exactly track the reference.

The repetitive controller ensures a precise tracking of the selected harmonics, and it provides the reference for the inner loop. In it, a PI controller improves the stability of the system, offering a low-pass filter function. The PI controller G_c is

$$G_c(S) = K_p + \frac{K_i}{s} \quad \text{.....(7)}$$

designed to ensure that the low-frequency poles have a damping factor of 0.707. The open-loop Bode diagram of the system is shown in Fig. 5.3(b): stability is guaranteed since the phase margins about 45◦. In normal operation mode, the shunt-connected converter injects the surplus of active power in the utility grid, and at the same time, it is controlled in order to cancel the harmonics of the load voltage. At low irradiation, the PV inverter only acts as a shunt controller, eliminating the harmonics. Controlling the voltage V_c , the PV converter is improved with the function of voltage dip compensation. In the presence of a voltage dip, the grid current I_g is forced by the controller to have a sinusoidal waveform that is phase shifted by 90◦ with respect to the corresponding grid voltage.

3.3 MPPT Algorithm

The power supplied from a PV array mostly depends on the present atmospheric conditions (irradiation and temperature); therefore, in order to collect the maximum available power, The operating point needs to continuously be tracked using an MPPT algorithm . To find the maximum power point (MPP) for all conditions, an MPPT control method based on the incremental conductance method which can tell on which side of the PV characteristic the current operating point is, has been used. The MPPT algorithm modifies the phase displacement between the grid voltage and the converter voltage, providing the voltage reference V_{ref}.

Furthermore, there is an extra feature added to this algorithm that monitors the maximum and minimum values of power oscillations on the PV side. In case of single-phase systems, the instant power oscillates with twice the line frequency. This oscillation in power on the grid side leads to a 100-Hz ripple in voltage and power on the PV side. If the system operates in the area around the MPP, the ripple of the power on the PV side is minimized . This feature can be used to detect in which part of the power–voltage characteristics the system operates. It happens in the proposed control scheme where information about the power oscillation can be used to find out how close the current operating point is to the MPP, thereby slowing down the increment of the reference, in order not to cross the MPP.

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

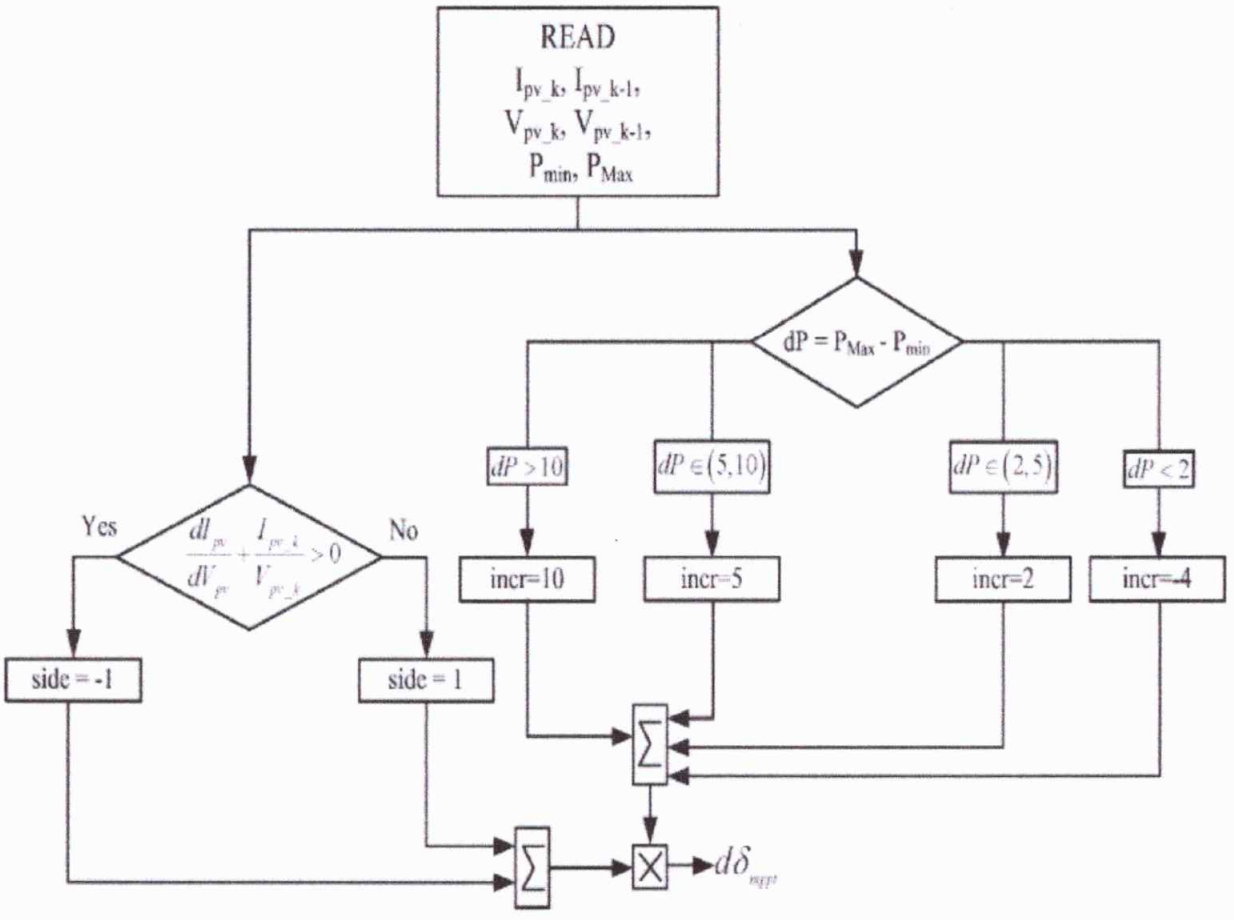


Fig 5.4 Flow chart of modified MPPT algorithm

A flowchart of the MPPT algorithm is shown in Fig.5.4 explaining how the angle of the reference voltage is modified in order to keep the operating point as close to MPP as possible. The MPP can be tracked by comparing the instantaneous conductance Ipv_k/Vpv_k to the incremental conductance dIpv/dVpv, as shown in the flowchart. Considering the power–voltage characteristic of a PV array, it can be observed that, operating in the area on the left side of the MPP, dδ mppt has to decrease. This decrement is indicated in Fig. 7 with *side* = −1. Moreover, operating in the area on the right side of the MPP, dδ mppt has to increase, and it is indicated with *side* = +1. The increment size determines how fast the MPP is tracked. The measure of the power oscillations on the PV side is used to quantify the increment that is denoted with increment in Fig.5.4.

The total energy production by the PV system daily for five months has been collected; the amount of energy generated by the PV system is changing from one day to another this is due to weather changes i.e., during cloudy and raining day. The average monthly energy production by

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

the PV system is shown in Figure . During the month of April, the PV system generates the highest level of energy for the sun.

The MPP tracking process is shown in Figure. The starting points vary, depending on the atmospheric condition, while the modulation index is changed continuously, resulting in the system steady-state operation around the maximum power point. The proposed MPPT was implemented in two different stages. The first stage senses the output voltage and current, digitaliize them using the ADC .The digital values are then used by the Genie software to generate the modulation index which is used as input to Xilinx FPGA to generate the required PWM in the second stage.

Photovoltaic power is an established technology and has recently experienced rapid growth over the last ten years . Photovoltaic cells are the key component in most photovoltaic power systems, but their performance is still subpar,so future work is needed to improve their performance and optimize the interactions between the cells and other components. The purpose of this paper is to investigate how to improve the control of the power interface and optimize the operation of the overall system. In a 24-h day, sunlight is only available for a limited time and depends heavily on weather conditions. In most photovoltaic power systems, a particular control algorithm, namely maximum power point tracking (MPPT), is utilized to take ful advantage of the available solar energy. Thus, the direction of this paper is to develop topologies for MPPT systems in order to more efficiently use harvested solar energy. Two principal types of photovoltaic power systems exist, which are classified by their functions and configuration, namely: 1) stand-alone systems and 2) grid-connected systems. The operation of stand-alone photovoltaic systems is independent of the electric utility grid. Recently, there have been an increasing number of grid-connected systems, which are in parallel with the electric utility grid and supply solar power to the utility via the grid. Ninety-three percent of the solar power systems installed in 2004 are grid-connected structure.

The operation of MPPT is to adjust photovoltaic interfaces so that the operating characteristics of the load and the photovoltaic array match at the maximum power point (MPP) no matter what the stand-alone or grid-connected photovoltaic application, which are numerous.This paper first investigates how partial shading affects the performance of MPPT and solar power generation. Second, it discusses topologies used for the optimization of MPPT of photovoltaic power systems. This paper presents two system structures suitable for photovoltaic features and MPPT. Finally,it gives a comparative study to select the best converter topology for photovoltaic interfaces.

4. Simulation Model

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

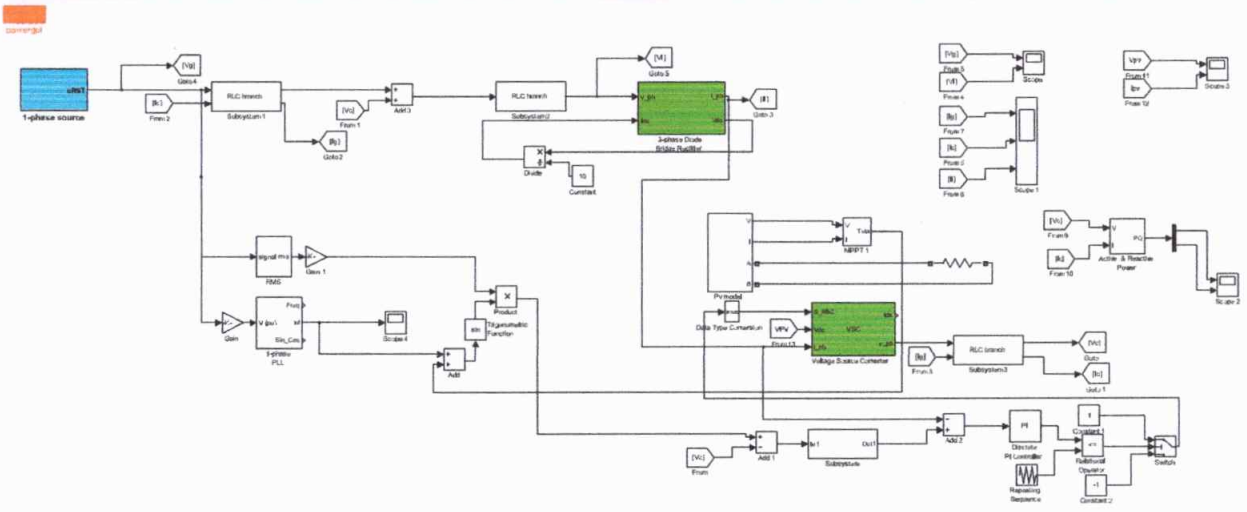


Fig 4.1 Simulation Model

4.1 MPPT Model

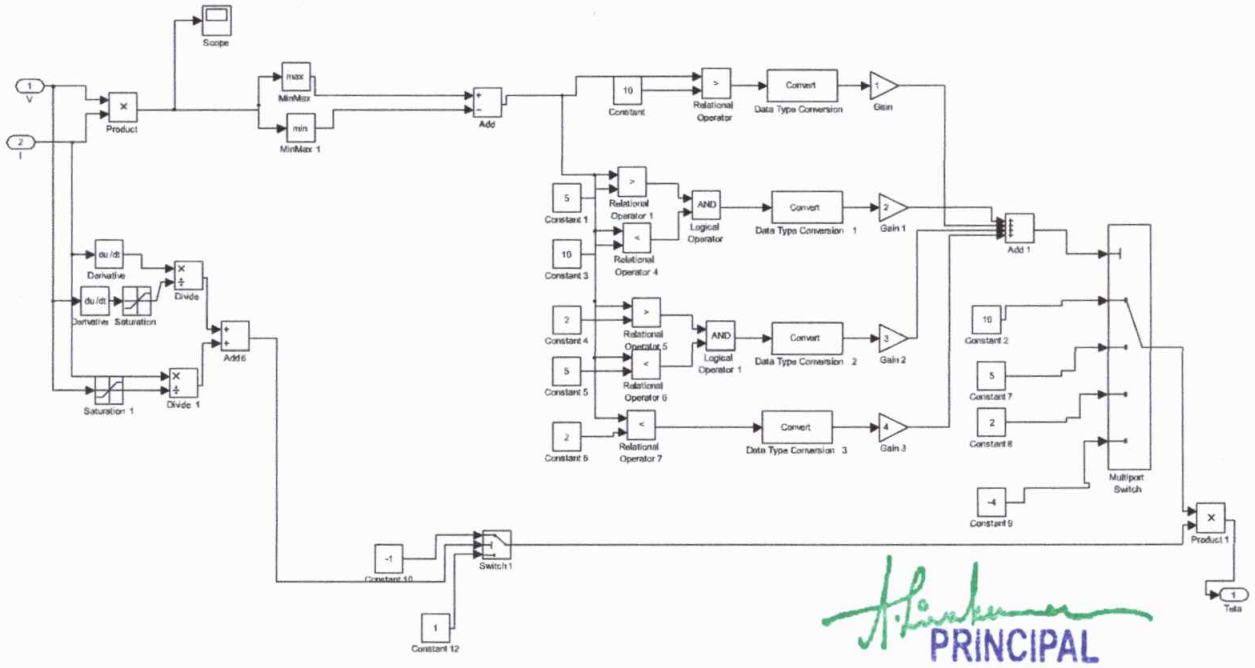
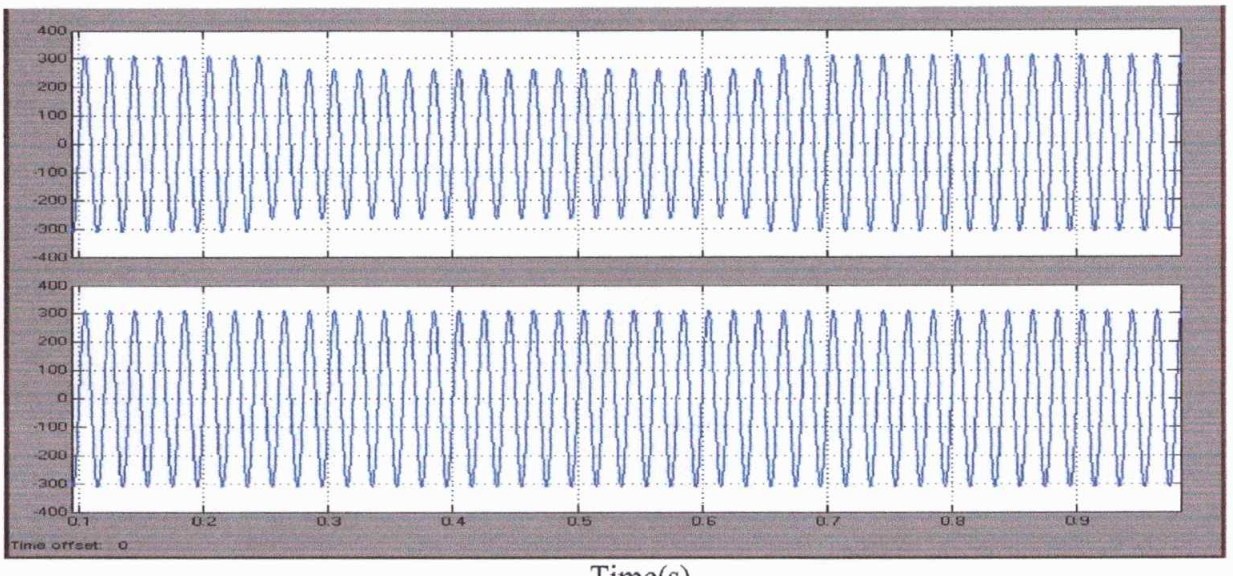


Fig 4.2 MPPT Model

4.2 Results of Voltage Controlled shunt converter with MPPT Algorithm

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS



Time(s)

Fig4.3 Performance of the voltage controlled shunt converter with MPPT Algorithm: grid voltage E, load voltage $V_{load.}$

4.3 Results of Grid Current Ig Converter current Ic Load current I_{load}

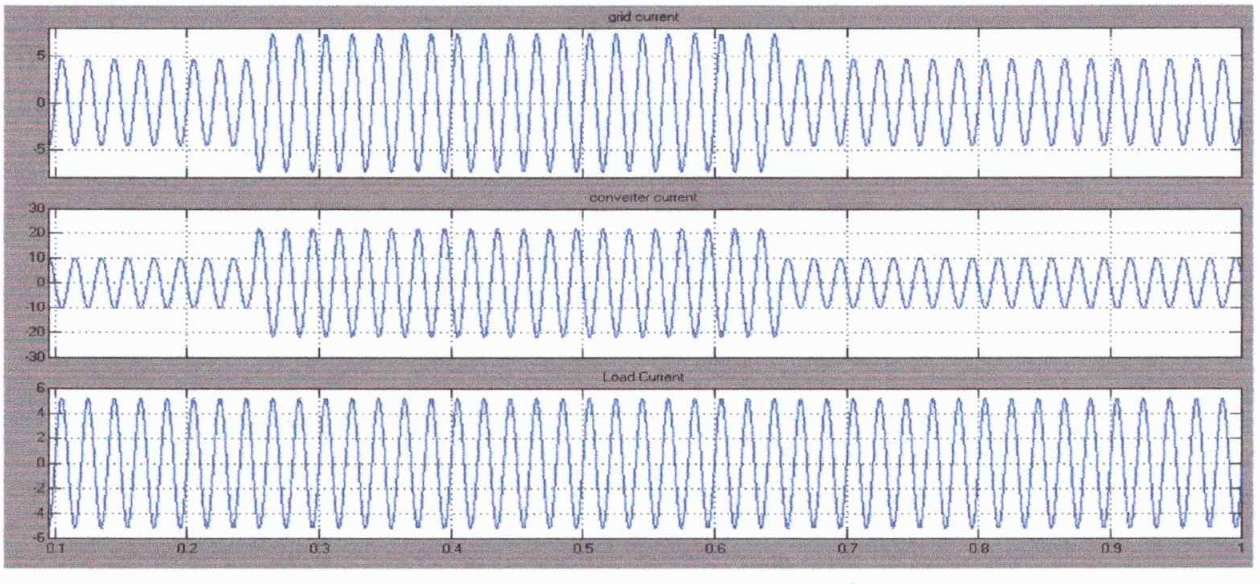


Fig 4.4 Performance of the voltage controlled shunt converter with MPPT Algorithm: grid current Ig, converter current Ic, load current $I_{load.}$

4.4 Results Of Active & Reactive Powers With Shunt Connected Converter

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

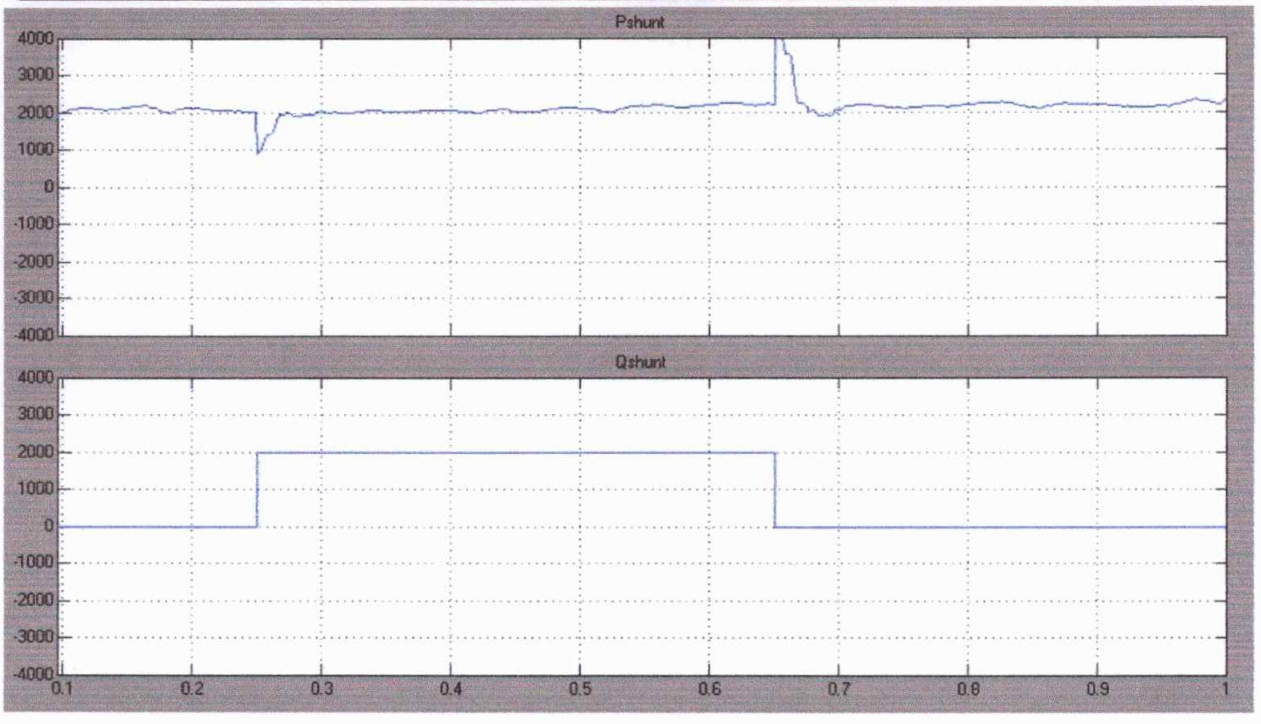


Fig 4.5 Active and reactive power provided by the shunt-connected Multifunctional converter to compensate the voltage sag of 0.15 pu.

4.5 Results of power voltage characteristics

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

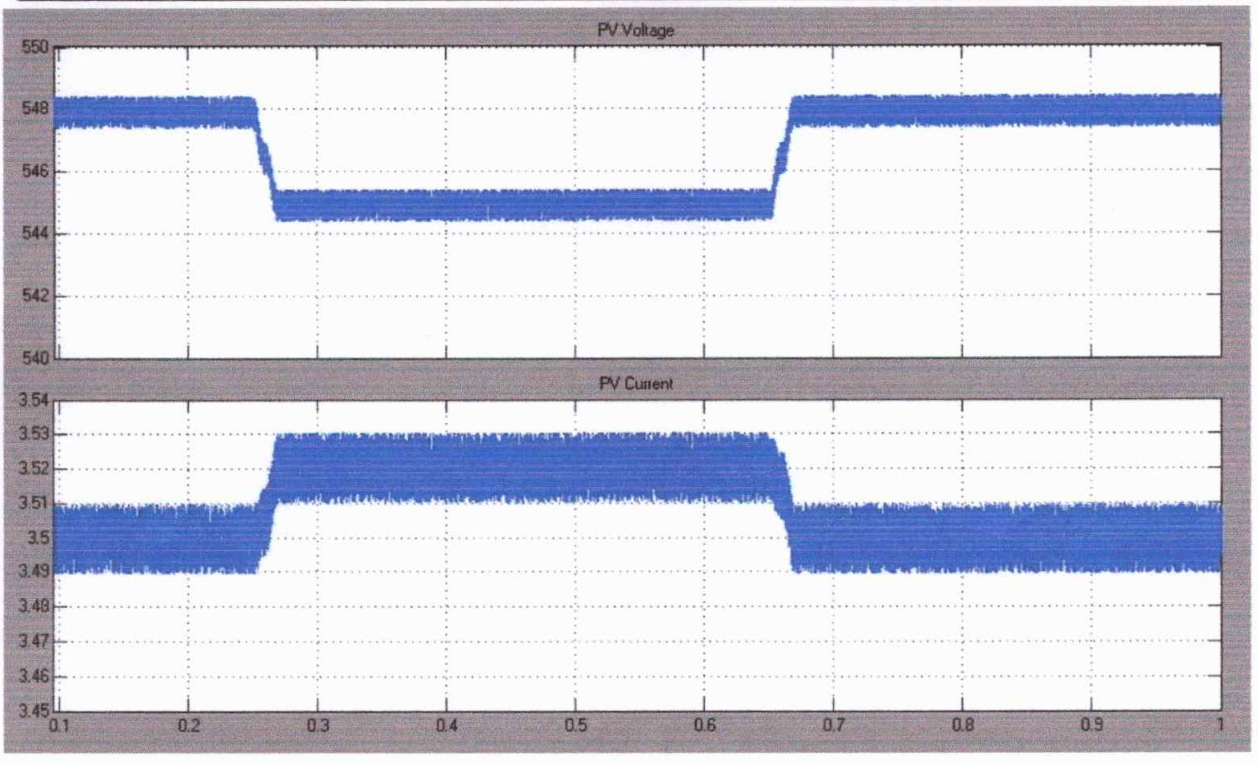


Fig 4.6 Power-voltage characteristic of the PV array and current and voltage on the PV side in presence of a grid voltage sag to 0.85 pu.

5. CONCLUSION

A single-phase PV system with shunt controller functionality has been presented. The PV converter is voltage controlled with a repetitive algorithm. An MPPT algorithm has specifically been designed for the proposed voltage-controlled converter. It is based on the incremental conductance method, and it has been modified to change the phase displacement between the grid voltage and the converter voltage maximizing the power extraction from the PV panels. The designed PV system provides grid voltage support at fundamental frequency and compensation of harmonic distortion at the point of common coupling. An inductance is added on the grid side in order to make the grid mainly inductive (it may represent the main drawback of the proposed system). Experimental results confirm the validity of the proposed solution in case of voltage dips and nonlinear load .

REFERENCES

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

1. F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," IEEE Trans. Ind. Electron., vol. 53,no. 5, pp. 1398–1409, Oct. 2006.
2. F. Blaabjerg, R. Teodorescu, Z. Chen, and M. Liserre, "Power converters and control of renewable energy systems," in Proc. ICPE, Pusan, Korea, Oct. 2004.
3. T.-F. Wu, H. S. Nien, H.-M. Hsieh, and C.-L. Shen, "PV power injection and active power filtering with amplitude-clamping and amplitude scaling algorithms," IEEE Trans. Ind. Appl., vol. 43, no. 3, pp. 731–741, May/Jun. 2007.
4. M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "On-line grid impedance estimation based onharmonic injection for grid-connected PV inverter," in Proc. IEEE Int. Symp. Ind. Electron., Jun.4–7, 2007, pp. 2437–2442.
5. IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems, IEEE Std. 1547-2003, 2003.
6. IEEE Guide for Monitoring, Information Exchange, and Control of Distributed Resources Interconnected With Electric Power Systems, IEEE Std. 1547.3-2007, 2007.
7. J. M. Guerrero, J. Matas, L. García de Vicuña, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed-generation inverters," IEEE Trans. Ind.Electron.,vol. 53, no. 5, pp. 1461–1470, Oct. 2006.
8. J. M. Guerrero, J. Matas, L. García de Vicuña, M. Castilla, and J. Miret, "Decentralized control for parallel operation of distributed generation inverters using resistive output impedance," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 994–1004, Apr. 2007.
9. K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen, and R. Belmans, "A voltage and frequency droop control method for parallel inverters," IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1107– 1115, Jul. 2007.
10. M. Bollen, Understanding Power Quality Problems: Voltage Sags and Interruptions. Piscataway, NJ: IEEE Press, 1999.
11. M. H. J. Bollen and I. Gu, Signal Processing of Power Quality Disturbances. New York: Wiley, 2006.
12. H. Kömürgügil and Ö. Kükrer, "A new control strategy for single-phase shunt active power filters using a Lyapunov function," IEEE Trans. Ind. Electron., vol. 53, no. 1, pp. 305–312, Feb.2006.
13. M. E. Ortúzar, R. E. Carmi, J. W. Dixon, and L. Morán, "Voltagesource active power filter based on multilevel converter and ultracapacitor ultracapacitor DC link," IEEE Trans. Ind. Electron., vol. 53, no. 2, pp. 477–485, Apr. 2006.
14. B.-R. Lin and C.-H. Huang, "Implementation of a three-phase capacitorclamped active power filter under unbalanced condition," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1621–1630, Oct. 2006.
15. I. Exteberria-Otadui, A. López de Heredia, H. Gaztañaga, S. Bacha, and M. R. Reyero, "A single synchronous frame hybrid (SSFH) multifrequency controller for power active filters,"IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1640–1648, Oct. 2006.

International
Journals & Magazines
ISSN No: 2248-9278/NOV-DEC19/ Vol-8/Issue-2
RESEARCH ARTICLE OPEN ACCESS

16. G. Escobar, P. Mattavelli, A. M. Stakovis, A. A. Valdez, and J. Leyva-Ramos, "An adaptive control for UPS to compensate unbalance and harmonic distortion using a combined capacitor/load current sensing," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 839–847, Apr. 2007.
17. D. O. Abdeslam, . Wira, J. Mercklé, D. Flieller, and Y.-A. Chapuis, "A unified artificial neural network architecture for active power filters," IEEE Trans. Ind. Electron., vol. 54, no. 1,pp. 61–76, Feb. 2007.

18. M. Routimo, M. Salo, and H. Tuusa, "Current sensorless control of a voltage-source active power filter," in Proc. 20th IEEE Annu. APEC, Mar. 6–10, 2005, vol. 3, pp. 1696–1702.
19. P. Wang, N. Jenkins, and M. H. J. Bollen, "Experimental investigation of voltage sag mitigation by an advanced static VAr compensator," IEEE Trans. Power Del., vol. 13, no. 4, pp.1461–1467, Oct. 1998.
20. P. Mattavelli and F. Pinhabel Marafao, "Repetitive-based control for selective harmonic compensation in active power filter," IEEE Trans. Ind. Electron., vol. 51, no. 5, pp. 1018–1024, Oct. 2004.
21. F. Botterón and H. Pinehiro, "A three-phase UPS that complies with the standard IEC 62040-3," IEEE Trans. Ind. Electron., vol. 54, no. 4,pp. 2120–2136, Aug. 2007.
22. G. Escobar, A. A. Valdez, J. Leyva-Ramos, and P. Mattavelli, "Repetitive basedcontroller for a UPS inverter to compensate unbalance and harmonic distortion," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 504–510, Feb. 2007.

PRINCIPAL
Avanthi Institute of Engg. & Tech
Guntihapally (V), Abdullapurmet (Mdl) R.R.Dist